DRAM

3.3V SDR SDRAM

A complete offering from 16Mbit to 512Mbit

► ISSI SDR Standard Features:

- Single supply voltage of 3.3V ± 0.3V
- Standard SDRAM clock timing
- LVTTL compatible inputs
- Four internal banks with bank controls[2]
- Data masking per byte on Read or Write commands
- Programmable burst length of 1, 2, 4, 8, or full page
- Programmable CAS Latency of 2 or 3
- Auto-Refresh and Self-Refresh Modes
- Auto-Precharge Supported
- JEDEC compliant:
  54-ball BGA or 54-pin TSOP-II for x16[2]
  90-ball BGA or 86-pin TSOP-II for x32

► Applications:

- Wireless Access Points
- Base Stations
- Routers
- Network Storage
- Energy Management
- Industrial Controls
- Car Infotainment
- Automotive Telematics

Key Timing Parameters

Speed (Max Freq.)	-5	-6	-7	-75E	Units
CL = 3	200	166	143	–	MHz
CL = 2	100	100	100	133	MHz

Note: These are general specs. For any given part number, please refer to the corresponding datasheet for the timing specifications.

ISSI SDR Ordering Options

Density	Config.	Part Number [1,3]	Package		Temperature Grade		
			TSOP2	BGA	Com.	Ind.	Auto.
16Mbit	1M x 16	IS42S16100H	■	■	■	■	■
64Mbit	4M x 16	IS42S16400N	■	■	■	■	■
	2M x 32	IS42S32200N	■	■	■	■	■
128Mbit	16M x 8	IS42S81600J	■		■	■	■
	8M x 16	IS42S16800J	■	■	■	■	■
	4M x 32	IS42S32400J	■	■	■	■	■
256Mbit	32M x 8	IS42S83200J	■	■	■	■	■
	16M x 16	IS42S16160J	■	■	■	■	■
	8M x 32	IS42S32800J	■	■	■	■	■
512Mbit	64M x 8	IS42S86400F	■		■	■	■
	32M x 16	IS42S16320F	■	■	■	■	■
	16M x 32	IS42S32160F	■	■	■	■	■

Notes:
1. Automotive grade SDR part numbers begin with "IS45S".
2. 16Mbit has two internal banks and JEDEC packaging is different.