IS61/64WV5128EFALL
IS61/64WV5128EFBLL

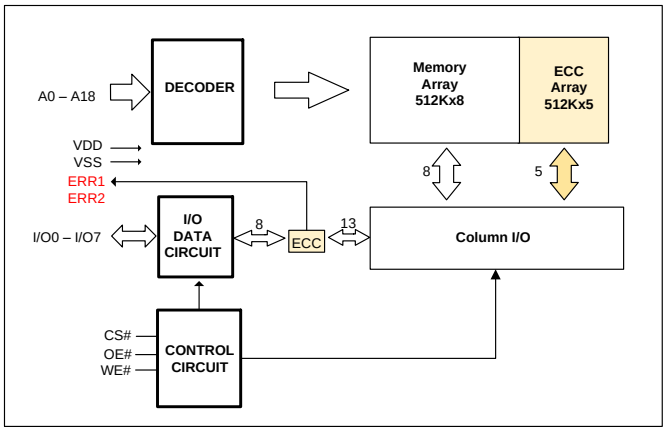
APRIL 2018

512Kx8 HIGH SPEED AYNCHRONOUS CMOS STATIC RAM with ECC

KEY FEATURES

- High-speed access time: 8ns, 10ns, 12ns
- Single power supply
  - 1.65V-2.2V VDD(IS61/64WV5128EFALL)
  - 2.4V-3.6V VDD (IS61/64WV5128EFBLL)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
  - ERR1 pin indicates 1-bit error detection and correction.
  - ERR2 pin indicates 2-bit error detection
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The *ISSI* IS61/64WV5128EFALL/EFBLL are high-speed, low power, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yield high-performance and highly reliable devices.

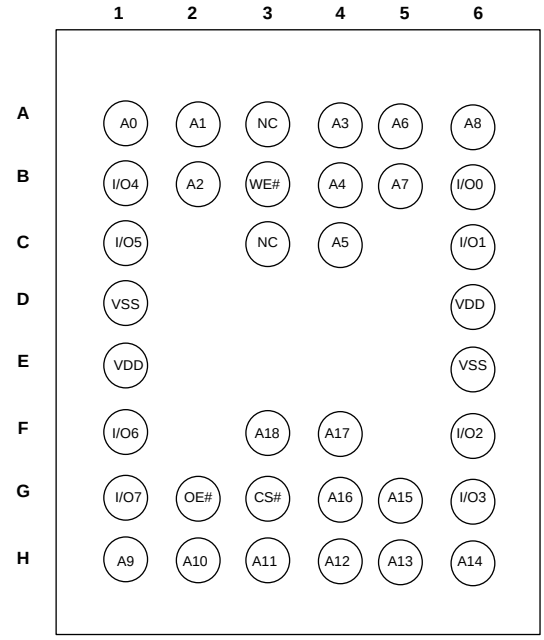
When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

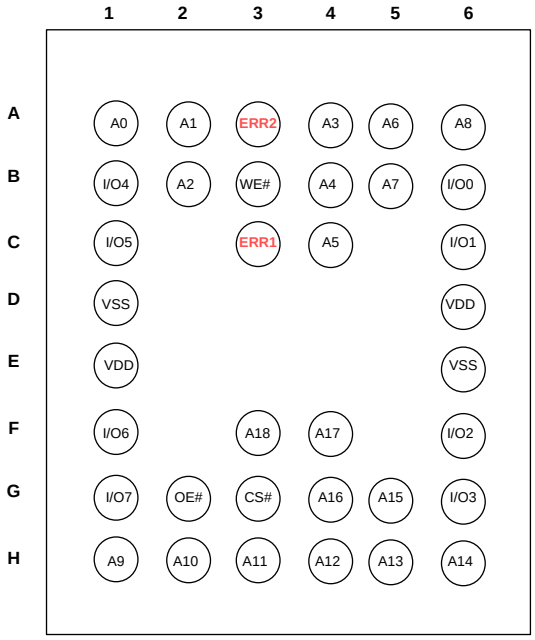
The IS61/64WV5128EFALL/EFBLL are packaged in the JEDEC standard 44-pin TSOP (TYPE II), 36-pin SOJ and 36-ball mini BGA (6mm x 8mm).

PIN CONFIGURATIONS

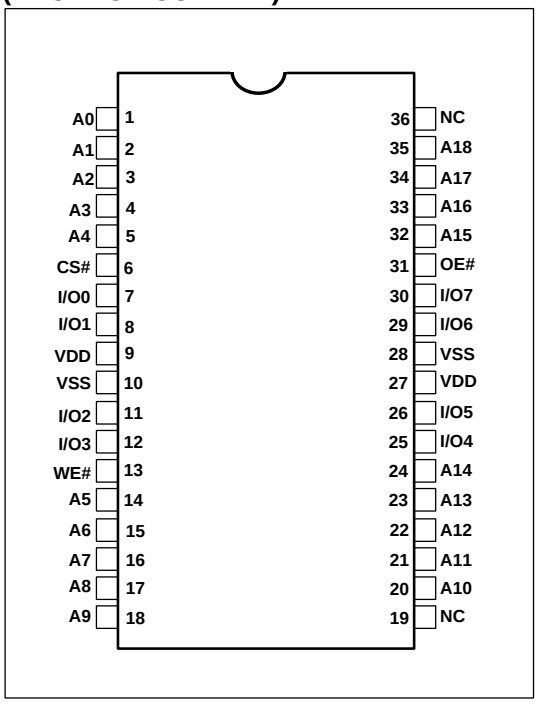
36-Ball mini BGA (6mm x 8mm) (Package Code: B)



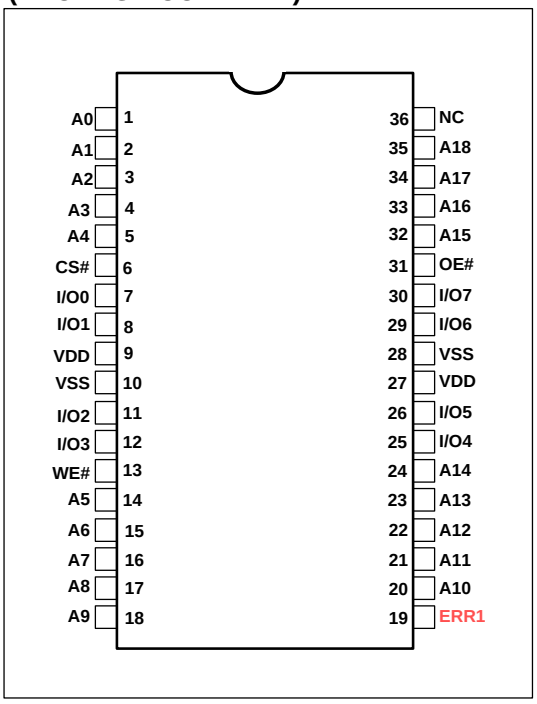
36-Ball mini BGA (6mm x 8mm), ERR1/2 (Package Code: B2)



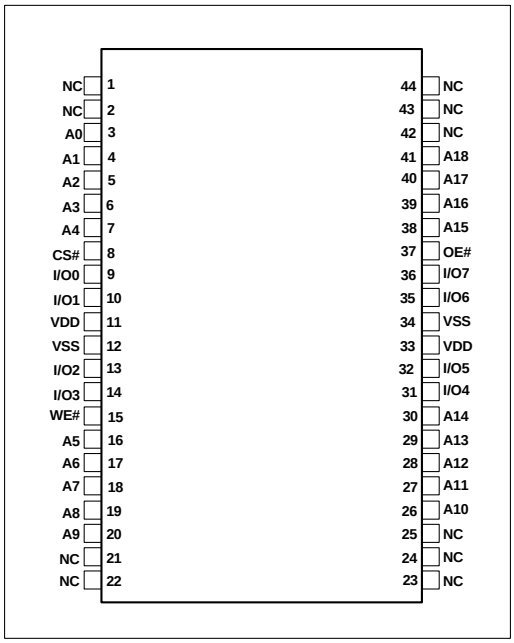
36-Pin SOJ (PACKAGE CODE : K)



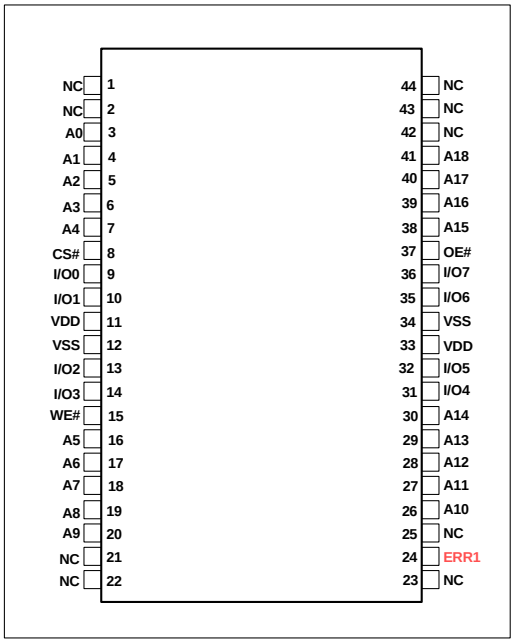
36-Pin SOJ, ERR1 (PACKAGE CODE : K2)



44-Pin TSOP (Type II)
(PACKAGE CODE : T)



44-Pin TSOP (Type II), ERR1
(PACKAGE CODE : T2)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O7	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
ERR1	1-bit Error Detection and Correction Signal
ERR2	2-bit ERR Detection Signal
NC	No Connection
V_{DD}	Power
VSS	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-7) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS#) and Write Enable (WE#) input LOW. The input and output pins (I/O0-7) are in data input mode. Output buffers are closed during this time even if OE# is LOW.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted.
In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct one bit error per byte or detect 2-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates 2-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

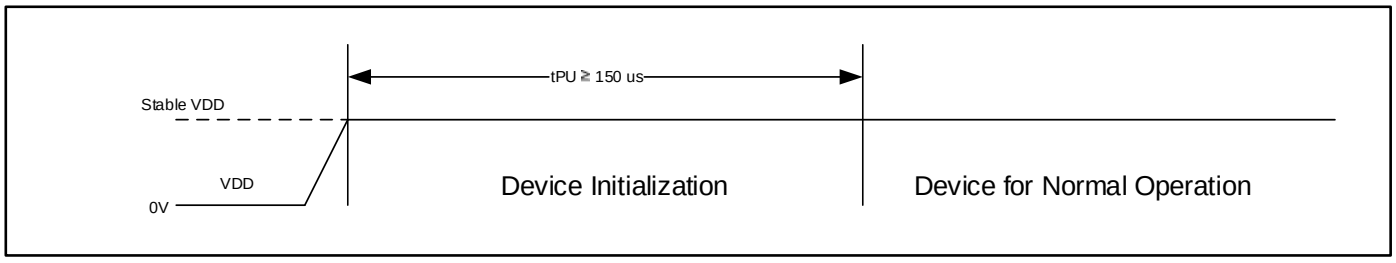
ERR1	ERR2	DQ pin	Status	Remark
0	0	Valid Q	No Error	
1	0	Valid Q	1-Bit Error only	1-bit error per byte detected and corrected
0	1	In-Valid Q	2-Bit Error only	No 1-bit error. 2-bit error per byte detected (out of 2 bytes)
1	1	In-Valid Q	1-bit & 2-bit error	1-bit error detected and corrected at one byte, and 2-bit error detected at another byte.
High-Z	High-Z	Valid D	Non-Read	Write operation or Output Disabled

TRUTH TABLE

Mode	CS#	WE#	OE#	I/O Operation	VDD Current
Not Selected	H	X	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	L	H	H	High-Z	ICC,ICC1
Read	L	H	L	DOUT	ICC,ICC1
Write	L	L	X	DIN	ICC,ICC1

POWER UP INITIALIZATION

The device includes on-chip voltage sensor used to launch POWER-UP initialization process.
When VDD reaches stable level, the device requires 150us of tPU (Power-Up Time) to complete its self-initialization process.
When initialization is complete, the device is ready for normal operation.



ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO7)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	VDD	SPEED (MAX)
Commercial	0°C to +70°C	IS61WV5128EFALL	1.65V – 2.2V	10 ns
		IS61WV5128EFBLL	2.4V – 3.6V	
			3.3V+/-10%	8ns
Industrial	-40°C to +85°C	IS61WV5128EFALL	1.65V – 2.2V	10 ns
		IS61WV5128EFBLL	2.4V – 3.6V	
			3.3V+/-10%	8ns
Automotive (A3)	-40°C to +125°C	IS64WV5128EFALL	1.65V – 2.2V	10 ns
		IS64WV5128EFBLL	2.4V – 3.6V	

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.4V~3.6V)	Unit (3.3V +/-10%)
Input Pulse Level	0V to V_{DD}	0V to V_{DD}	0V to V_{DD}
Input Rise and Fall Time	1.5 ns	1.5 ns	1.5 ns
Output Timing Reference Level	½ V_{DD}	½ V_{DD}	½ V_{DD}
R1 (ohm)	13500	319	319
R2 (ohm)	10800	353	353
V_{TM} (V)	V_{DD}	V_{DD}	V_{DD}
Output Load Conditions	Refer to Figure 1 and 2		

AC TEST LOADS

FIGURE 1

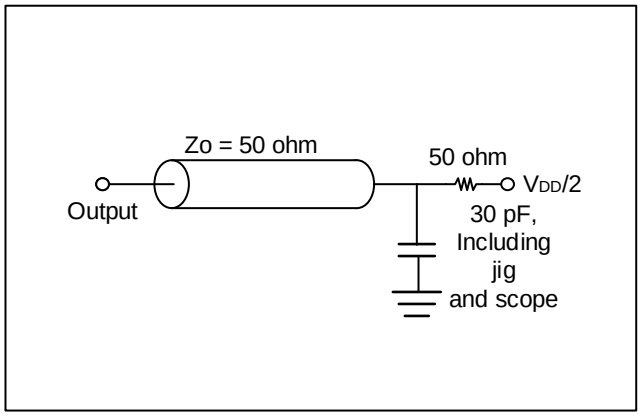
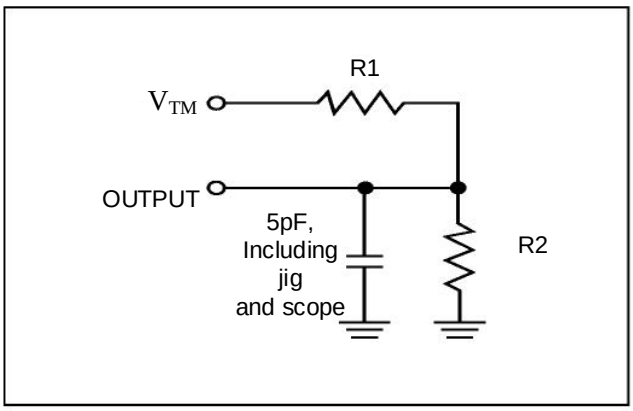


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (OVER THE OPERATING RANGE)

IS61/64WV5128EFALL (VDD = 1.65V – 2.2V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Note:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS61/64WV5128EFBLL (VDD = 2.4V – 3.6V)

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OH} = -1.0 mA	2.0	—	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OH} = -4.0 mA	2.2		
V_{OL}	Output LOW Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OL} = 2.0 mA	—	0.4	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	
V_{IH}(1)	Input HIGH Voltage	2.4V ~ 2.7V		2.0	V_{DD} + 0.3	V
		2.7V ~ 3.6V		2.0		
V_{IL}(1)	Input LOW Voltage	2.4V ~ 2.7V		–0.3	0.6	V
		2.7V ~ 3.6V		–0.3	0.8	
I_{LI}	Input Leakage		VSS < V_{IN} < V_{DD}	–2	2	µA
I_{LO}	Output Leakage		VSS < V_{IN} < V_{DD}, Output Disabled	–2	2	µA

Note:
1. VIL(min) = -0.3V DC ; VIL(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
   VIH (max) = VDD + 0.3V DC ; VIH(max) = VDD + 2.0V AC (pulse width 2.0ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-8[3] Max.	-10 Max.	-12 Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = f_{MAX}	Com.	40	30	30	mA
			Ind.	45	35	35	
			Auto.	-	40	40	
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	20	20	20	mA
			Ind.	25	25	25	
			Auto.	-	35	35	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL} CS# ≥ V_{IH}, f = 0	Com.	15	15	15	mA
			Ind.	20	20	20	
			Auto.	-	30	30	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	8	8	8	mA
			Ind.	10	10	10	
			Auto.	-	20	20	
			Typ. [2]	3			

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical value indicate the value for the center of distribution, measured at V_{DD} = 3.0V/1.8V, T_A = 25 °C, and not 100% tested.
3. 8ns is at VDD=3.3V +/-10%

AC CHARACTERISTICS (OVER OPERATING RANGE)

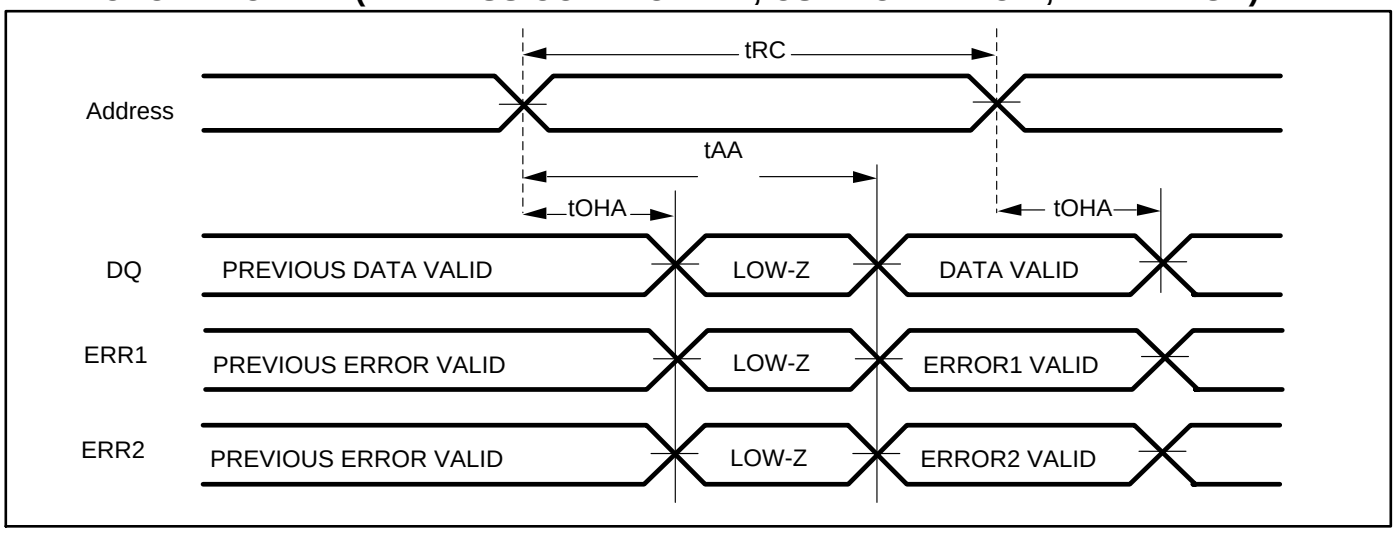
READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	-8[3]		-10		-12		unit	notes
		Min	Min	Min	Min	Min	Max		
Read Cycle Time	tRC	8	-	10	-	12	-	ns	
Address Access Time	tAA	-	8	-	10	-	12	ns	
Output Hold Time	tOHA	2.0	-	2.5	-	2.5	-	ns	
CS# Access Time	tACE	-	8	-	10	-	12	ns	
OE# Access Time	tDOE	-	4.5	-	6	-	7	ns	
OE# to High-Z Output	tHZOE	0	3	0	5	0	6	ns	2
OE# to Low-Z Output	tLZOE	0	-	0	-	0	-	ns	2
CS# to High-Z Output	tHZCE	0	3	0	5	0	6	ns	2
CS# to Low-Z Output	tLZCE	3	-	3	-	3	-	ns	2

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0V to V_{DD} and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. 8ns is at VDD=3.3V +/-10%

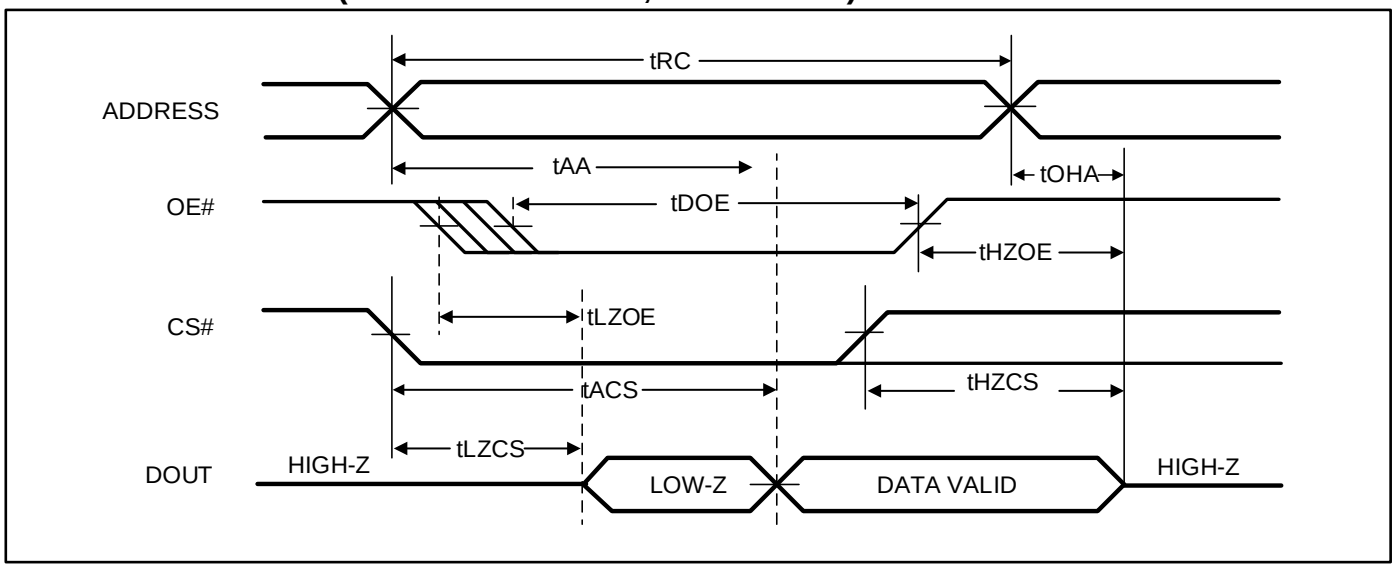
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED, CS# = OE# = LOW, WE# = HIGH)



Notes:
1. The device is continuously selected.
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

READ CYCLE NO. 2[1] (OE# CONTROLLED, WE# = HIGH)



Note:
1. Address is valid prior to or coincident with CS# LOW transition.

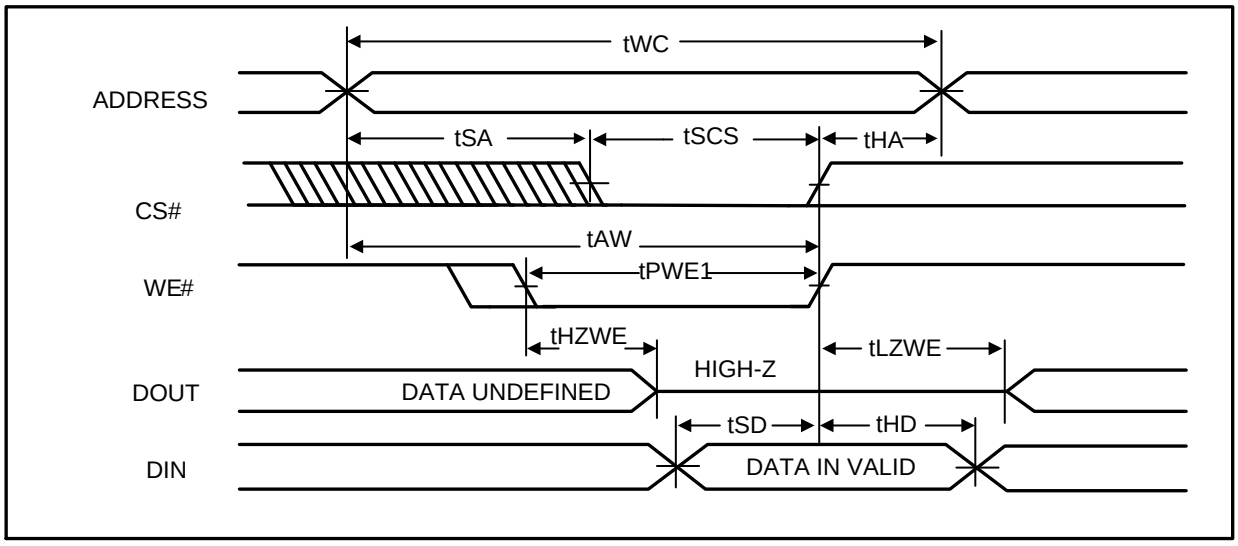
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-8[3]		-10		-12		unit	notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	tWC	8	-	10	-	12	-	ns	
CS# to Write End	tSCS	6.5	-	8	-	9	-	ns	
Address Setup Time to Write End	tAW	6.5	-	8	-	9	-	ns	
Address Hold from Write End	tHA	0	-	0	-	0	-	ns	
Address Setup Time	tSA	0	-	0	-	0	-	ns	
WE# Pulse Width	tPWE1	6.5	-	8	-	9	-	ns	
WE# Pulse Width (OE# = LOW)	tPWE2	8	-	10	-	12	-	ns	2
Data Setup to Write End	tSD	5	-	6	-	7	-	ns	
Data Hold from Write End	tHD	0	-	0	-	0	-	ns	
WE# LOW to High-Z Output	tHZWE	-	3.5	-	4	-	5	ns	
WE# HIGH to Low-Z Output	tLZWE	2	-	2	-	2	-	ns	

Notes:
1 The internal write time is defined by the overlap of CS# = LOW, and WE# = LOW. All conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2 tPWE > tHZWE + tSD when OE# is LOW.
3 8ns is at VDD=3.3V +/-10%

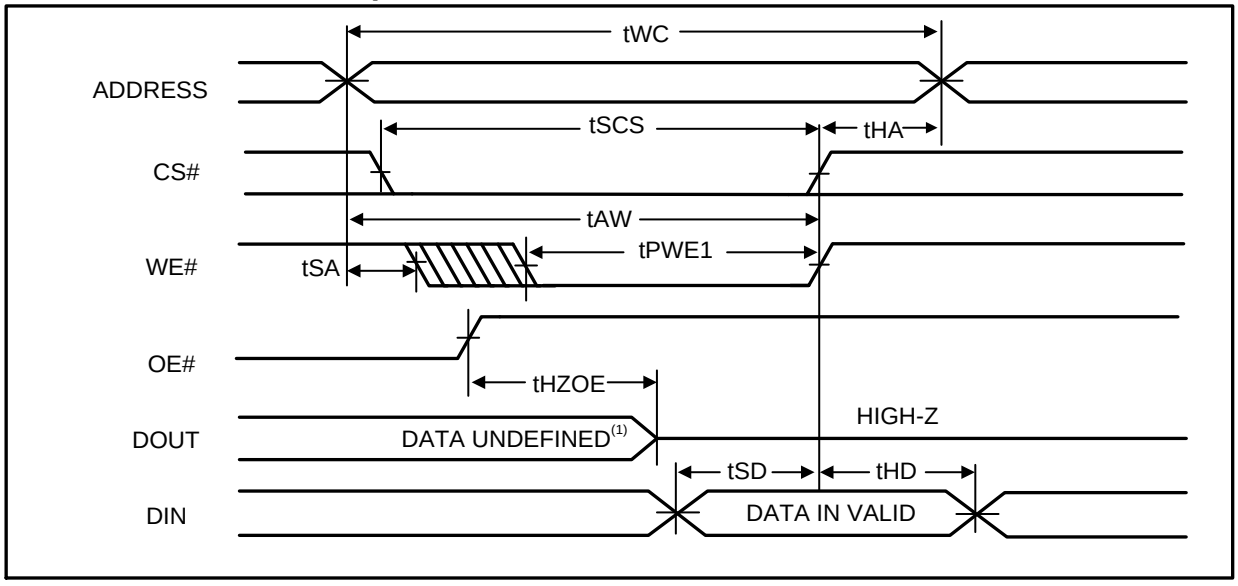
AC WAVEFORMS

WRITE CYCLE NO. 1[1] (CS# CONTROLLED, OE# = HIGH OR LOW)



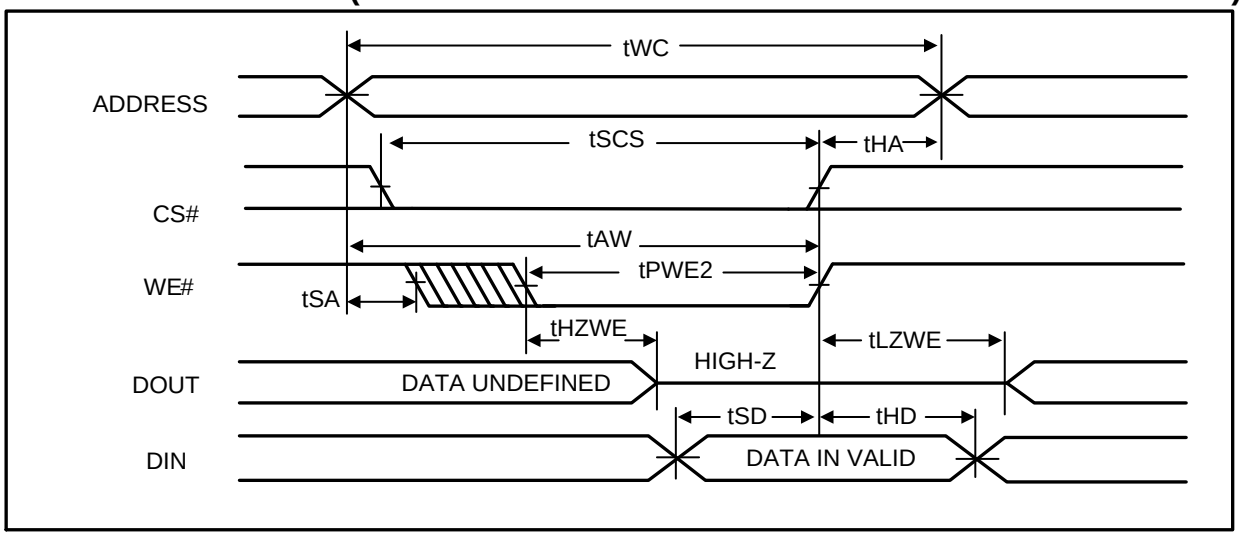
Note:
1. I/O will assume the High-Z state if CS# = V_{IH} or OE# = V_{IH}.

WRITE CYCLE NO. 2[1] (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



Note:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:

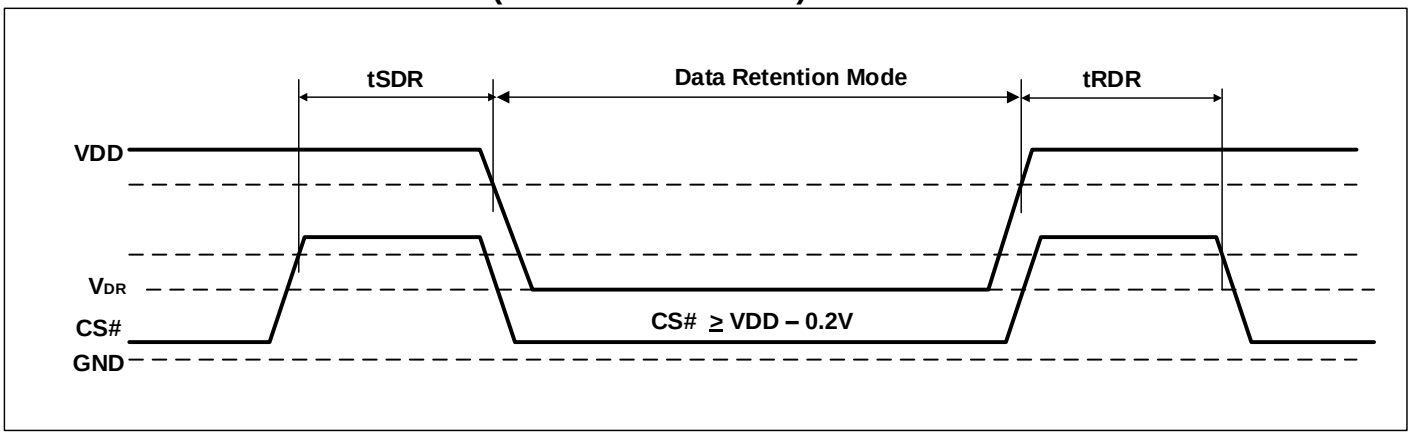
1. I/O will assume the High-Z state if CS# = V_{IH} or OE# = V_{IH}.

DATA RETENTION CHARACTERISTICS(2)

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	V_{DD} = 2.4V to 3.6V	2.0		-	V
			V_{DD} = 1.65V to 2.2V	1.2		-	
I_{DR}	Data Retention Current	V_{DD}= V_{DR} (min), CS# ≥ V_{DD} – 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	-	3 (1)	8	mA
			Ind.	-	-	10	
			Auto	-	-	20	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. Typical value indicates the value for the center of distribution, measured at V_{DD} = V_{DR} (min.), T_A = 25 °C and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C, Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
10	IS61WV5128EFALL-10BI	36-ball mini BGA (6mm x 8mm)
10	IS61WV5128EFALL-10BLI	36-ball mini BGA (6mm x 8mm), Lead-free
10	IS61WV5128EFALL-10B2I	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS61WV5128EFALL-10B2LI	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS61WV5128EFALL-10KLI	400-mil Plastic SOJ, Lead-free
10	IS61WV5128EFALL-10K2LI	400-mil Plastic SOJ, ERR1 Pin, Lead-free
10	IS61WV5128EFALL-10TLI	TSOP (Type II) , Lead-free
10	IS61WV5128EFALL-10T2LI	TSOP (Type II), ERR1 Pin , Lead-free

Industrial Range: -40°C to +85°C, Voltage Range: 2.4V to 3.6V

Speed (ns)[1]	Order Part No.	Package
10 (8)	IS61WV5128EFBLL-10BI	36-ball mini BGA (6mm x 8mm)
10 (8)	IS61WV5128EFBLL-10BLI	36-ball mini BGA (6mm x 8mm), Lead-free
10 (8)	IS61WV5128EFBLL-10B2I	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10 (8)	IS61WV5128EFBLL-10B2LI	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10 (8)	IS61WV5128EFBLL-10KLI	400-mil Plastic SOJ, Lead-free
10 (8)	IS61WV5128EFBLL-10K2LI	400-mil Plastic SOJ, ERR1 Pin, Lead-free
10 (8)	IS61WV5128EFBLL-10TLI	TSOP (Type II) , Lead-free
10 (8)	IS61WV5128EFBLL-10T2LI	TSOP (Type II), ERR1 Pin , Lead-free

Note:
1. Speed = 8ns when VDD = 3.3V +/-10%. Speed = 10ns when VDD = 2.4V to 3.6V

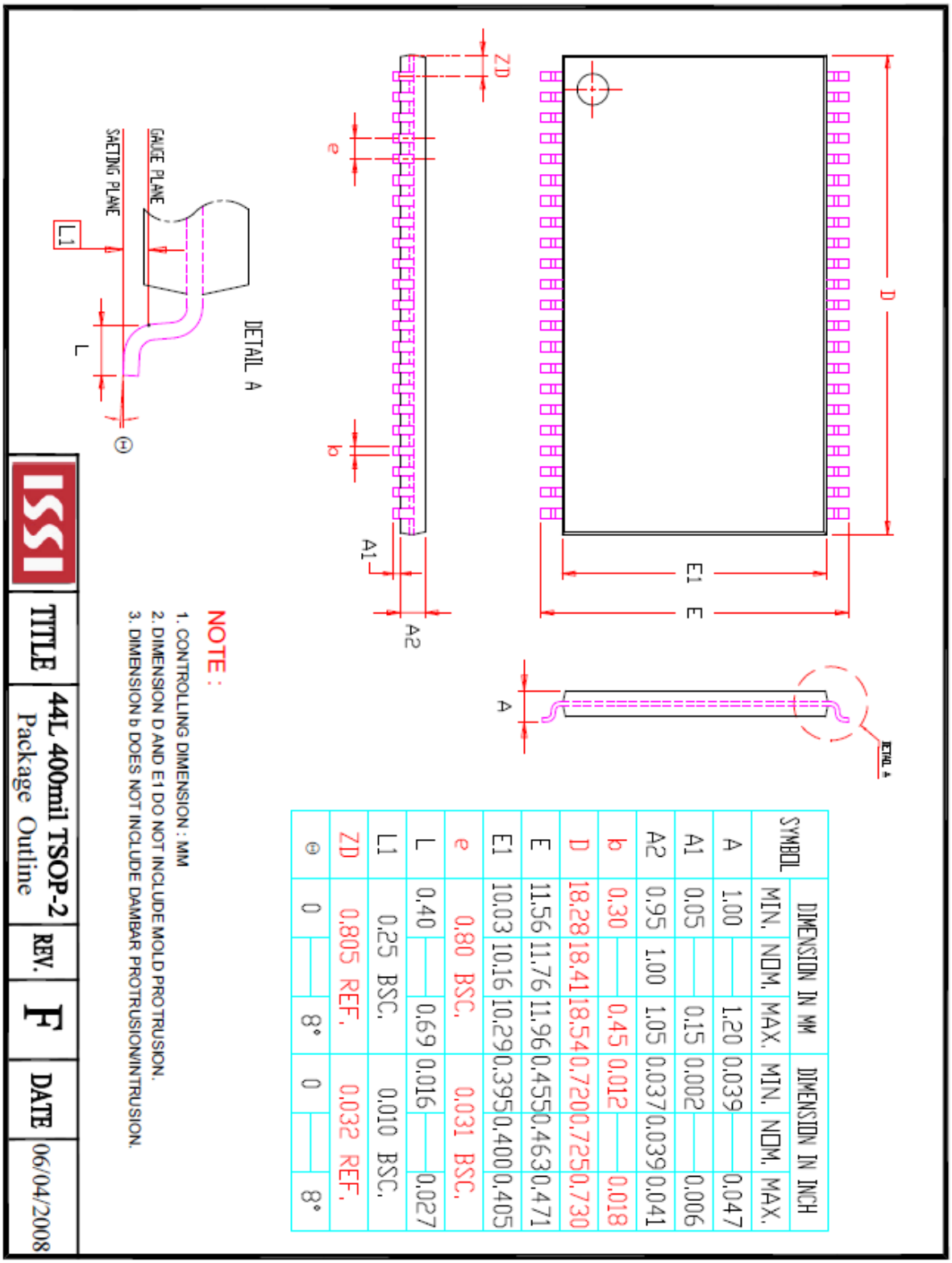
Automotive (A3) Range: –40°C to +125°C, Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
12	IS64WV5128EFALL-12BA3	36-ball mini BGA (6mm x 8mm)
12	IS64WV5128EFALL-12BLA3	36-ball mini BGA (6mm x 8mm), Lead-free
12	IS64WV5128EFALL-12B2A3	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV5128EFALL-12B2LA3	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV5128EFALL-12KLA3	400-mil Plastic SOJ, Lead-free
12	IS64WV5128EFALL-12K2LA3	400-mil Plastic SOJ, ERR1 Pin, Lead-free
12	IS64WV5128EFALL-12CTLA3	TSOP (Type II) , Lead-free
12	IS64WV5128EFALL-12CT2LA3	TSOP (Type II), ERR1 Pin , Lead-free

Automotive (A3) Range: –40°C to +125°C, Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV5128EFBLL-10BA3	36-ball mini BGA (6mm x 8mm)
10	IS64WV5128EFBLL-10BLA3	36-ball mini BGA (6mm x 8mm), Lead-free
10	IS64WV5128EFBLL-10B2A3	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS64WV5128EFBLL-10B2LA3	36-ball mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS64WV5128EFBLL-10KLA3	400-mil Plastic SOJ, Lead-free
10	IS64WV5128EFBLL-10K2LA3	400-mil Plastic SOJ, ERR1 Pin, Lead-free
10	IS64WV5128EFBLL-10CTLA3	TSOP (Type II) , Lead-free
10	IS64WV5128EFBLL-10CT2LA3	TSOP (Type II), ERR1 Pin , Lead-free

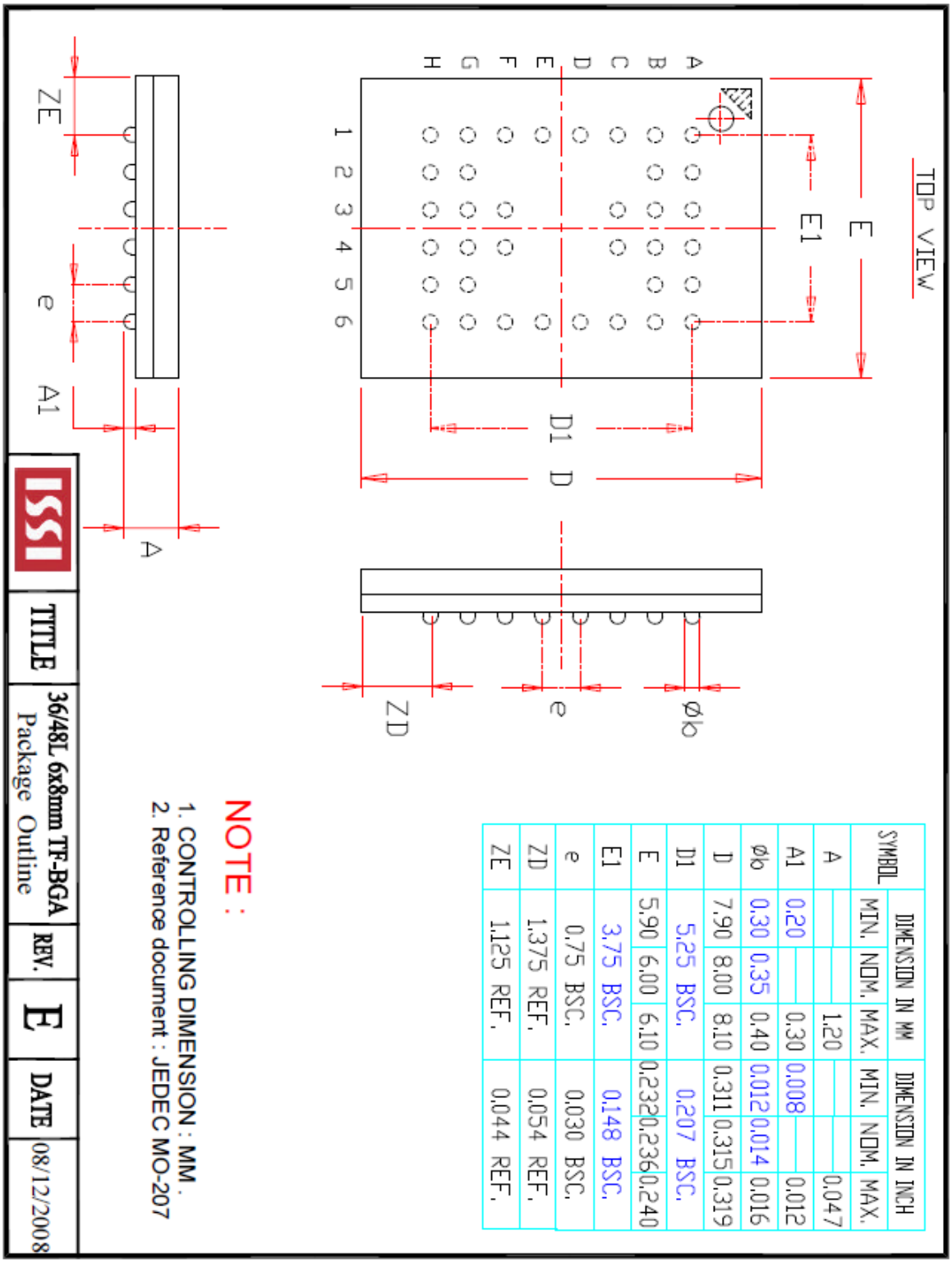
PACKAGE INFORMATION



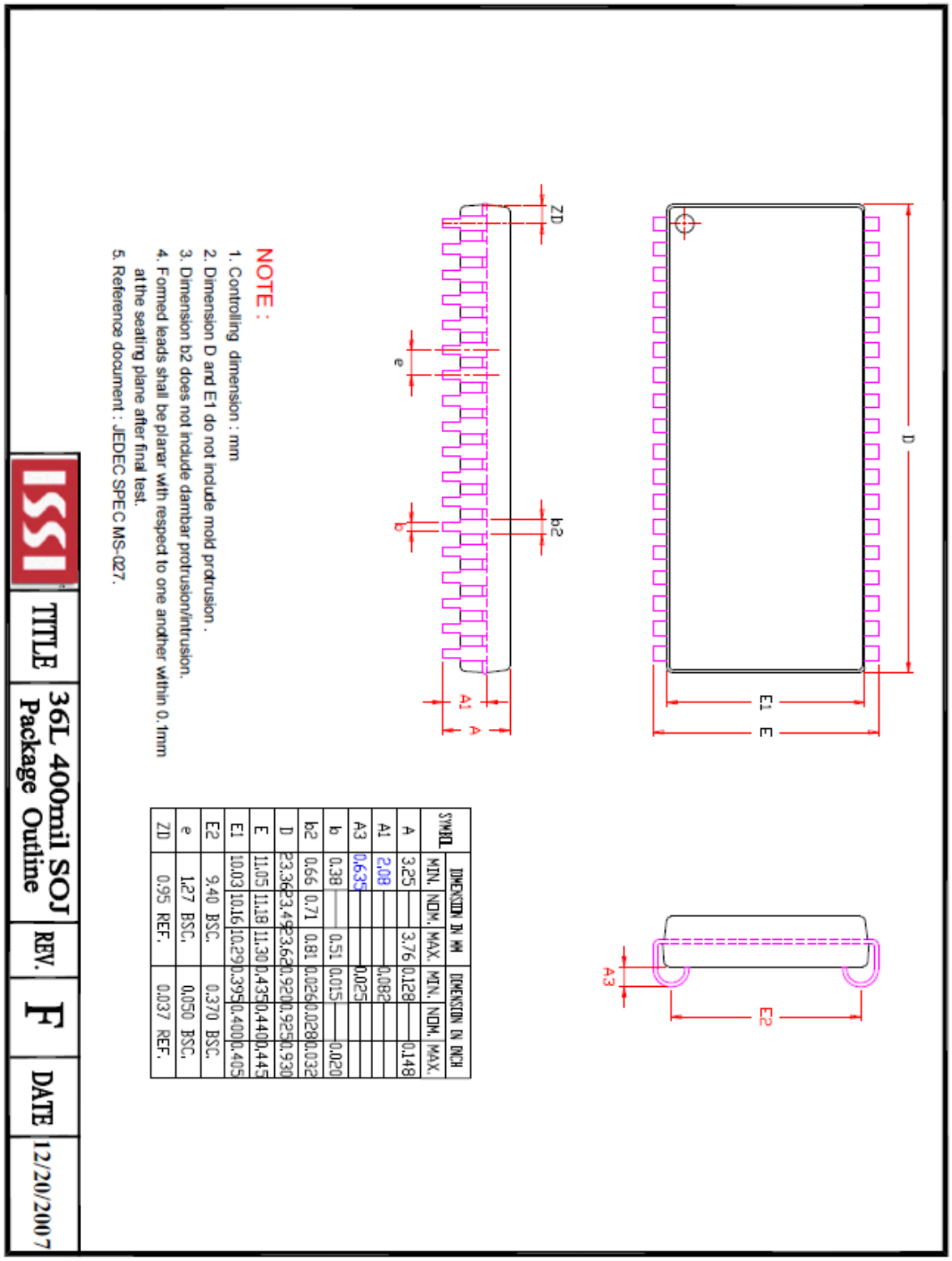
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		0.80 BSC.			0.031 BSC.	
L	0.40	—	0.69	0.016	—	0.027
L1		0.25 BSC.			0.010 BSC.	
ZD		0.805 REF.			0.032 REF.	
θ	0	—	8°	0	—	8°

NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE 06/04/2008



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		5.25 BSC.			0.207 BSC.	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		3.75 BSC.			0.148 BSC.	
e		0.75 BSC.			0.030 BSC.	
ZD		1.375 REF.			0.054 REF.	
ZE		1.125 REF.			0.044 REF.	



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	—	0.082	—	—
A3	0.635	—	—	0.025	—	—
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	23.36	23.49	23.62	0.920	0.925	0.930
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC.			0.370 BSC.		
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

TITLE	36L 400mil SOJ Package Outline	REV.	F	DATE	12/20/2007