FEBURARY 2020

512Kx8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  – Operating Current: 32 mA (max.)
  – CMOS Standby Current: 3.2 uA (typ., 25°C)
- TTL compatible interface levels
- Single power supply
  –1.65V-2.2V VDD (IS62/65WV5128EHALL)
  – 2.2V-3.6V VDD (IS62/65WV5128EHBLL)
- Optional ERR1/ERR2 pin:
  – ERR1: indicates 1-bit error detection and correction
  – ERR2: indicates 2-bit error detection
- Three state outputs
- Commercial, Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

The *ISSI* IS62/65WV5128EHALL/BLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability. This highly reliable process coupled with innovative circuit design techniques including ECC, yields high-performance and low power consumption devices.

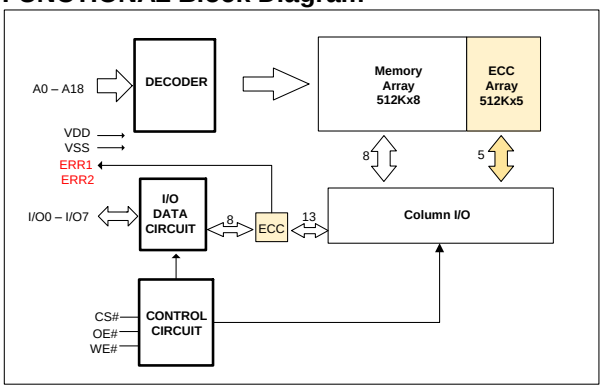
This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DEC: Single Error Correcting-Double Error Detecting), yields high performance and low power consumption devices.

When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

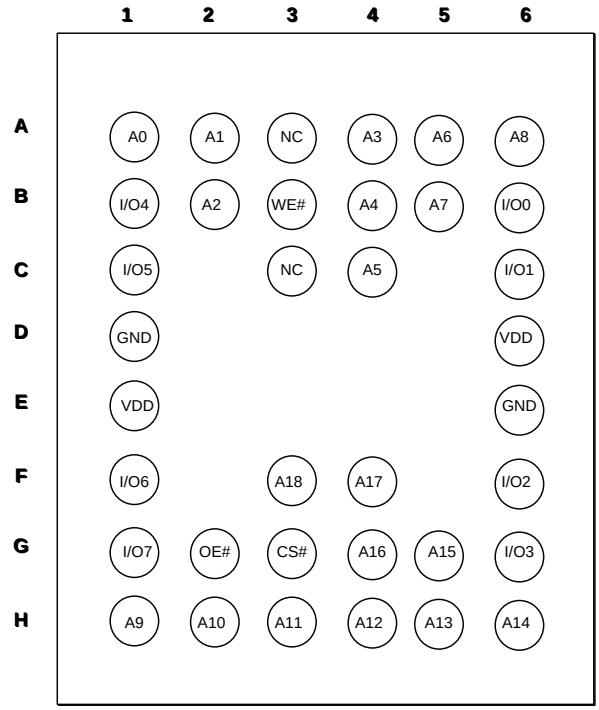
The IS62/65WV5128EHALL/BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I/II), sTSOP (TYPE I) and 36-pin mini BGA

FUNCTIONAL Block Diagram

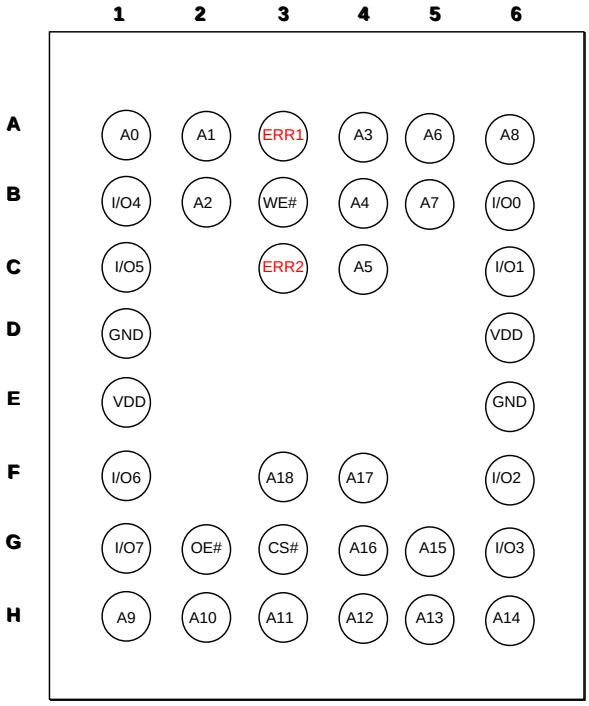


PIN CONFIGURATIONS

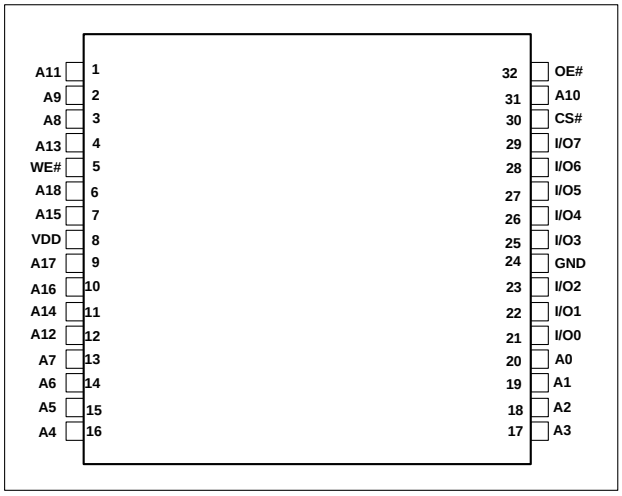
36-Pin mini BGA (6mm x 8mm)



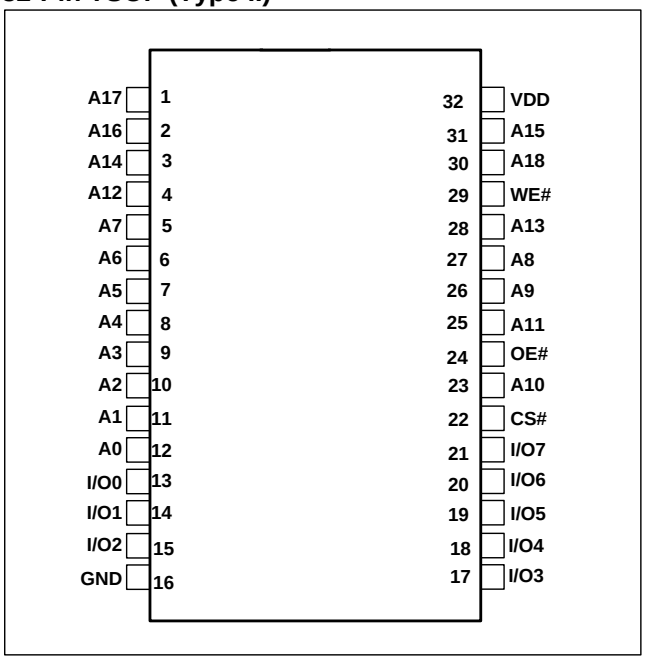
36-Pin mini BGA (6mm x 8mm), ERR1/2



32-Pin TSOP (Type I)
32-Pin STSOP (Type I)



32-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O7	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
ERR1	Single ERR Correction Signal
ERR2	Double ERR Detection Signal
NC	No Connection
V_{DD}	Power
GND	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-7) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input LOW. The input and output pins (I/O0-7) are in data input mode. Output buffers are closed during this time even if OE# is LOW.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct one bit error per byte or detect 2-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates 2-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1/2 OUTPUT SIGNAL BEHAVIOR

ERR1	ERR2	DQ pin	Status	Remark
0	0	Valid Q	No Error	
1	0	Valid Q	1-Bit Error only	1-bit error per byte detected and corrected
0	1	In-Valid Q	2-Bit Error	2-bit error per byte detected
High-Z	High-Z	Valid D	Non-Read	Write operation or Output Disabled

TRUTH TABLE

Mode	CS#	WE#	OE#	I/O0-I/O7	VDD Current
Not Selected	H	X	X	High-Z	ISB2
Output Disabled	L	H	H	High-Z	ICC,ICC1
Write	L	H	L	DIN	ICC,ICC1
Read	L	L	X	DOUT	ICC,ICC1

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.5 to 3.9 (V_{DD} + 0.3V)	V
V_{DD}	V_{DD} Related to GND	–0.3 to 3.9 (V_{DD} + 0.3V)	V
tStg	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD(MIN)	VDD(TYP)	VDD(MAX)
Commercial	0°C to +70°C	~ALL	55 ns	1.65V	1.8V	2.2V
Industrial	-40°C to +85°C		55 ns	1.65V	1.8V	2.2V
Automotive	-40°C to +125°C		55 ns	1.65V	1.8V	2.2V
Commercial	0°C to +70°C	~BLL	45ns	2.2V	3.0V	3.6V
Industrial	-40°C to +85°C		45ns	2.2V	3.0V	3.6V
Automotive	-40°C to +125°C		55ns	2.2V	3.0V	3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO7)	$C_{I/O}$		8	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.2V~3.6V)
Input Pulse Level	0V to V_{DD} -0.2V	0V to V_{DD} -0.3V
Input Rise and Fall Time	1V/ns	1V/ns
Output Timing Reference Level	0.9V	½ V_{DD}
R1	13500	1005
R2	10800	820
V_{TM}	1.8V	3.0V
Output Load Conditions	Refer to Figure 1 and 2	

OUTPUT LOAD CONDITIONS FIGURES

FIGURE 1

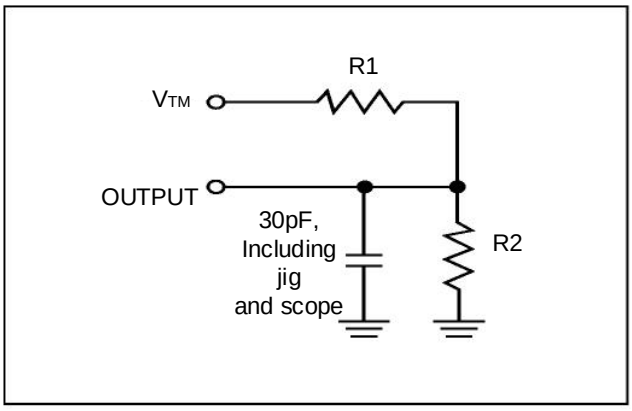
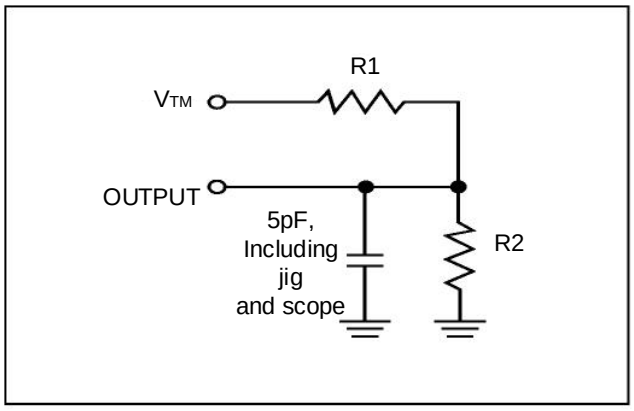


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS- I (OVER THE OPERATING RANGE)

2/65WV5128EHALL (VDD = 1.65V ~ 2.2V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Note:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS- I (OVER THE OPERATING RANGE)

IS62/65WV5128EHBLL (VDD = 2.2V ~ 3.6V)

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage		2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
			2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage		2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
			2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage		2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
			2.7 ≤ V_{DD} ≤ 3.6	2.0	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
			2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage		GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage		GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Note:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

IS62/65WV5128EHALL (VDD = 1.65V ~ 2.2V)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}$ (max), I_{OUT} = 0mA, f = f_{max}	Com.		-	32	mA
			Ind.		-	32	
			Auto. A3		-	32	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}$ (max), I_{OUT} = 0mA, f = 0	Com.		-	6	mA
			Ind.		-	6	
			Auto. A3		-	6	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}$ (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	25°C	3.2	6	µA
				40°C	3.4	8	
				70°C	5.0	11	
			Ind.	85°C	6.6	14	
			Auto. A3	125°C	18.0	35	

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD}=V_{DD} (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested.

DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

IS62/65WV5128EHBLL (VDD = 2.2V ~ 3.6V)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}$(max), I_{OUT} = 0mA, f = f_{max}	Com.		-	32	mA
			Ind.		-	32	
			Auto. A3		-	32	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}$(max), I_{OUT} = 0mA, f = 0	Com.		-	6	mA
			Ind.		-	6	
			Auto. A3		-	6	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}$ (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	25°C	3.2	6	µA
				40°C	3.4	8	
				70°C	5.0	11	
			Ind.	85°C	6.6	14	
			Auto. A3	125°C	18.0	35	

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD}=V_{DD} (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested.

AC CHARACTERISTICS(6) (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address, ERR Access Time	tAA	-	45	-	55	ns	1
Output, ERR Hold Time	tOHA	10	-	10	-	ns	1
CS# Access Time	tACS	-	45	-	55	ns	1
OE# Access Time	tDOE	-	20	-	25	ns	1
OE# to High-Z Output	tHZOE	-	15	-	20	ns	2
OE# to Low-Z Output	tLZOE	5	-	5	-	ns	2
CS# to High-Z Output	tHZCS	-	15	-	20	ns	2
CS# to Low-Z Output	tLZCS	10	-	10	-	ns	2

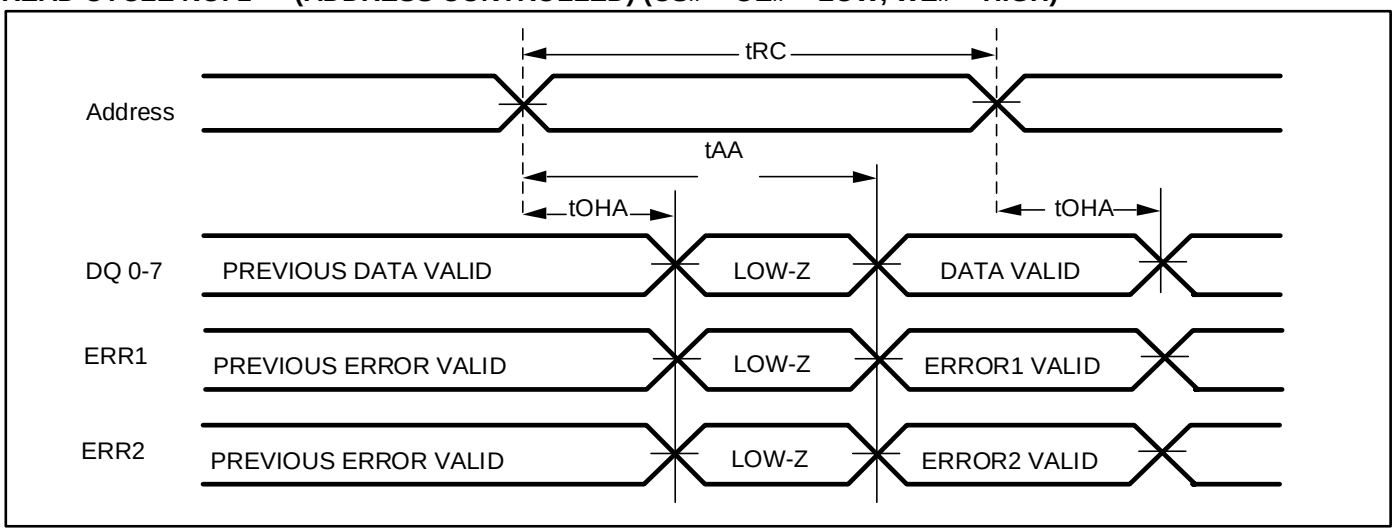
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Min		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
CS# to Write End	tSCS	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
WE# Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	20	-	25	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
WE# LOW to High-Z Output	tHZWE	-	15	-	20	ns	2,3
WE# HIGH to Low-Z Output	tLZWE	5	-	5	-	ns	2,3

Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS# = LOW, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS

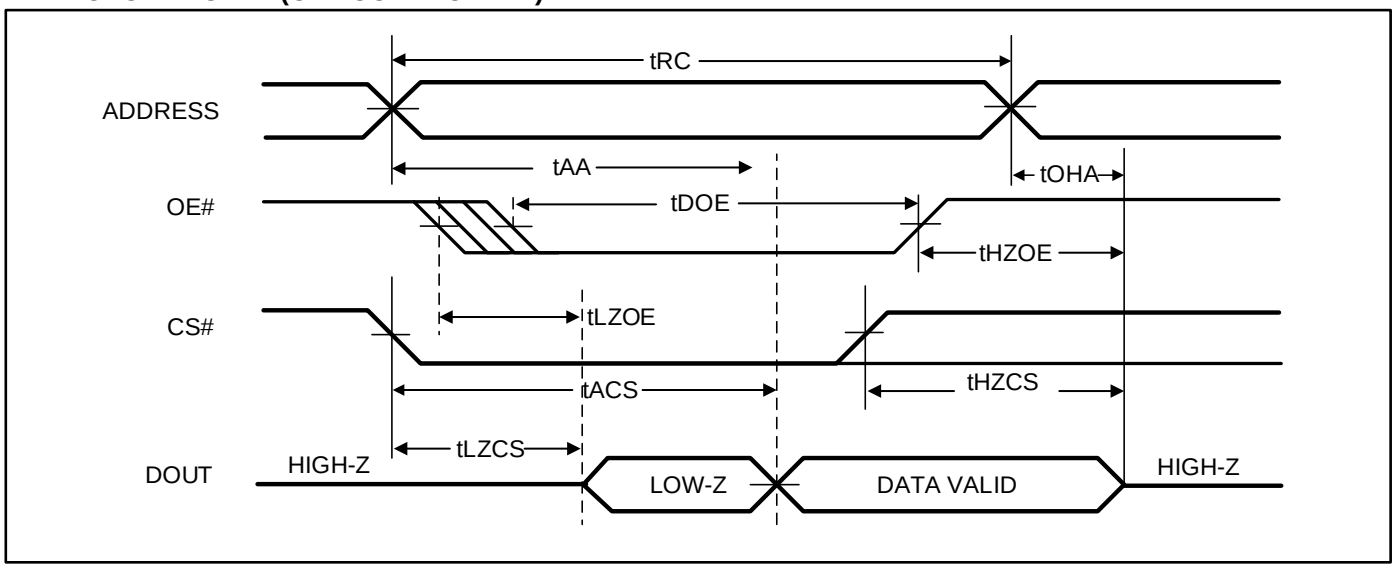
Timing Diagram

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED) (CS# = OE# = LOW, WE# = HIGH)



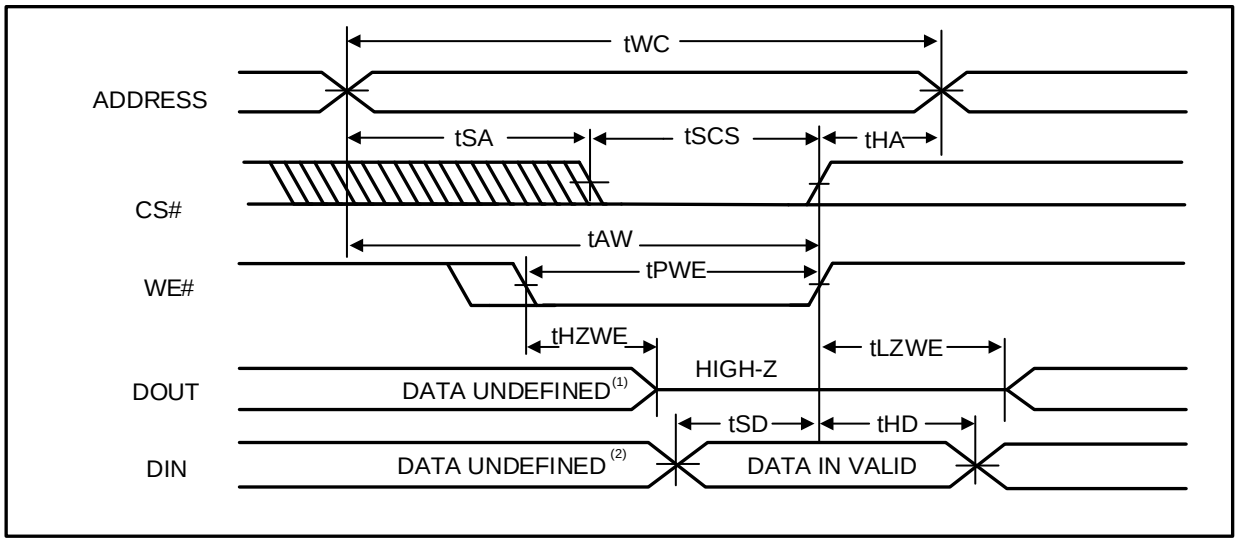
Notes:
1. The device is continuously selected
2. The ERR1,ERR2 signal acts like a Read Data Q during Read Operation.

READ CYCLE NO. 2[1] (OE# CONTROLLED)



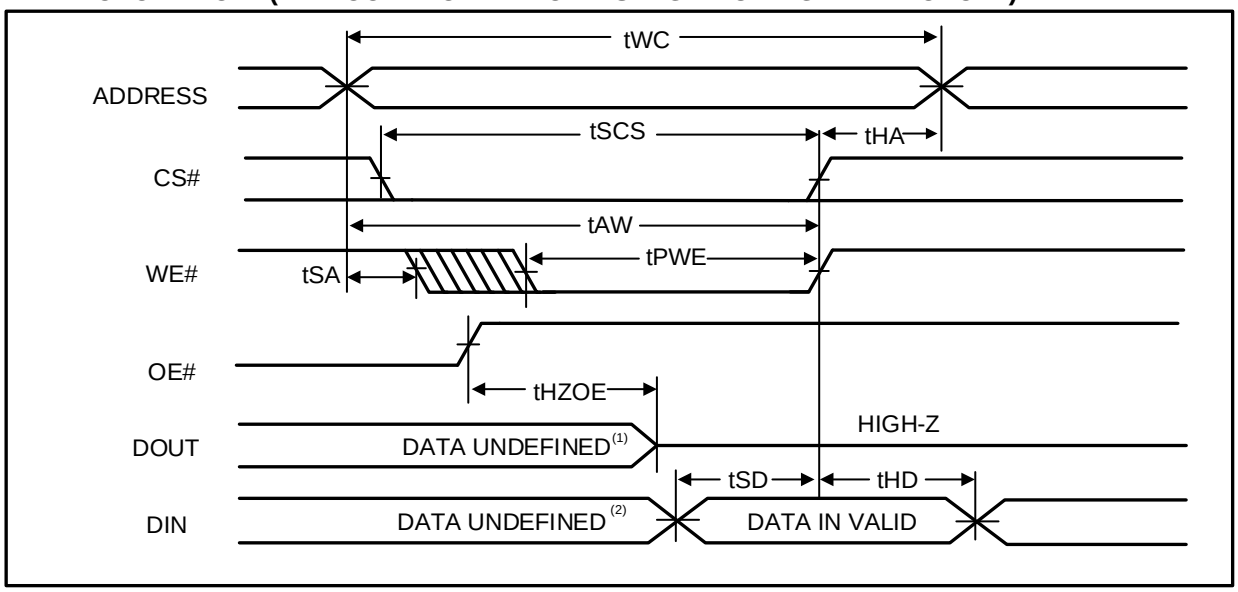
Notes:
1. Address is valid prior to or coincident with CS# LOW transition.

WRITE CYCLE 1[1, 2] (CS# Controlled, OE# = HIGH or LOW)



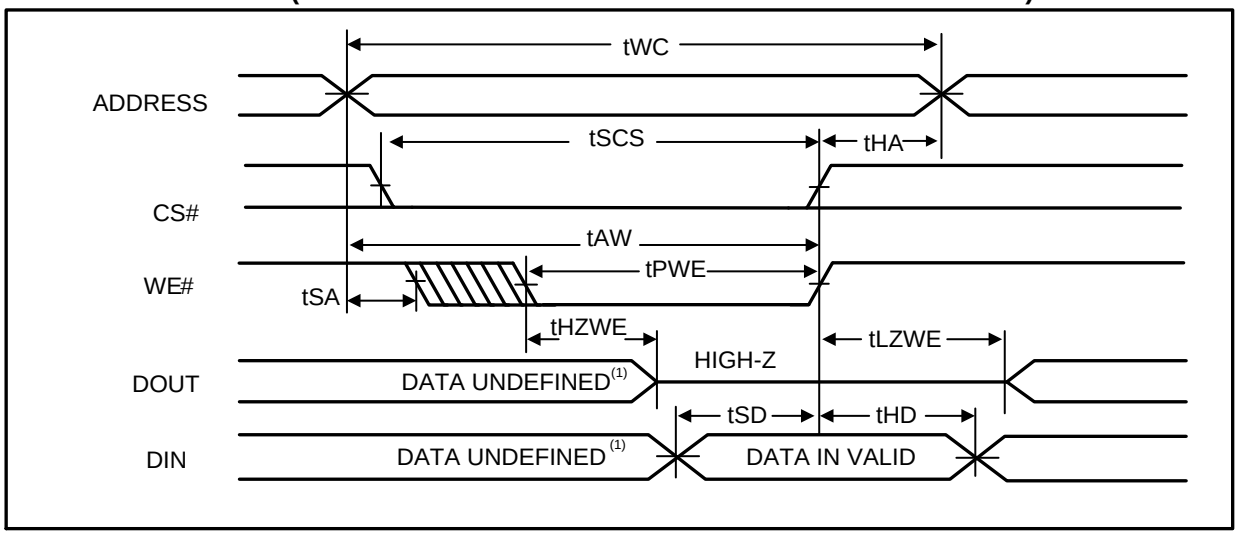
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2 (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



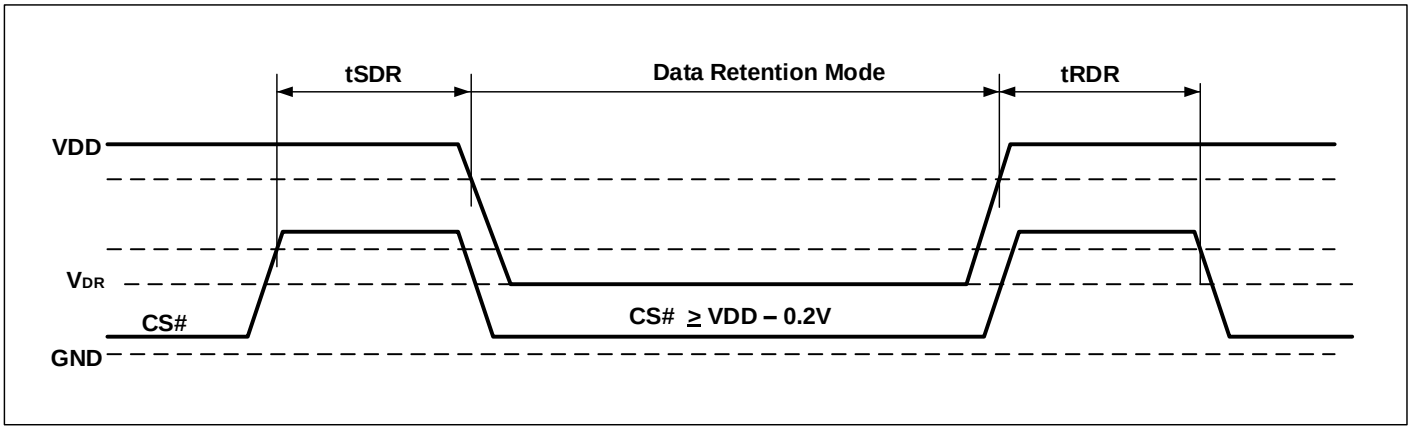
Note:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.5	-	-	V
I_{DR}	Data Retention Current	V_{DD} = MAX, CS1# ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	25°C	-	3.2	5.5	uA
			85°C	-	-	13	
			125°C	-	-	33	
t_{SDR} (2)	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD} = V_{DR} (min.), and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

IS62WV5128EHALL (1.65V - 2.2V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62WV5128EHALL-55TL	TSOP, Type I (8 x 20 mm), Lead-free
55	IS62WV5128EHALL-55T2L	TSOP, Type II, Lead-free
55	IS62WV5128EFALL-55HL	sTSOP (Type I), (8 x 13.4 mm), Lead-free
55	IS62WV5128EHALL-55B	mini BGA (6mm x 8mm)
55	IS62WV5128EHALL-55BL	mini BGA (6mm x 8mm), Lead-free
55	IS62WV5128EHALL-55B2	mini BGA (6mm x 8mm), ERR1/2
55	IS62WV5128EHALL-55B2L	mini BGA (6mm x 8mm), Lead-free, ERR1/2

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV5128EHALL-55TLI	TSOP, Type I (8 x 20 mm), Lead-free
55	IS62WV5128EHALL-55T2LI	TSOP, Type II, Lead-free
55	IS62WV5128EHALL-55HLI	sTSOP (Type I), (8 x 13.4 mm), Lead-free
55	IS62WV5128EHALL-55BI	mini BGA (6mm x 8mm)
55	IS62WV5128EHALL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV5128EHALL-55B2I	mini BGA (6mm x 8mm), ERR1/2
55	IS62WV5128EHALL-55B2LI	mini BGA (6mm x 8mm), Lead-free, ERR1/2

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

PLEASE CONTACT ISSI MARKETING

IS62WV5128EHBLL (2.2V – 3.6V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62WV5128EHBLL-45TL	TSOP, Type I (8 x 20 mm), Lead-free
45	IS62WV5128EHBLL-45T2L	TSOP, Type II, Lead-free
45	IS62WV5128EHBLL-45HL	sTSOP (Type I), (8 x 13.4 mm), Lead-free
45	IS62WV5128EHBLL-45B	mini BGA (6mm x 8mm)
45	IS62WV5128EHBLL-45BL	mini BGA (6mm x 8mm), Lead-free
45	IS62WV5128EHBLL-45B2	mini BGA (6mm x 8mm), ERR1/2
45	IS62WV5128EHBLL-45B2L	mini BGA (6mm x 8mm), Lead-free, ERR1/2

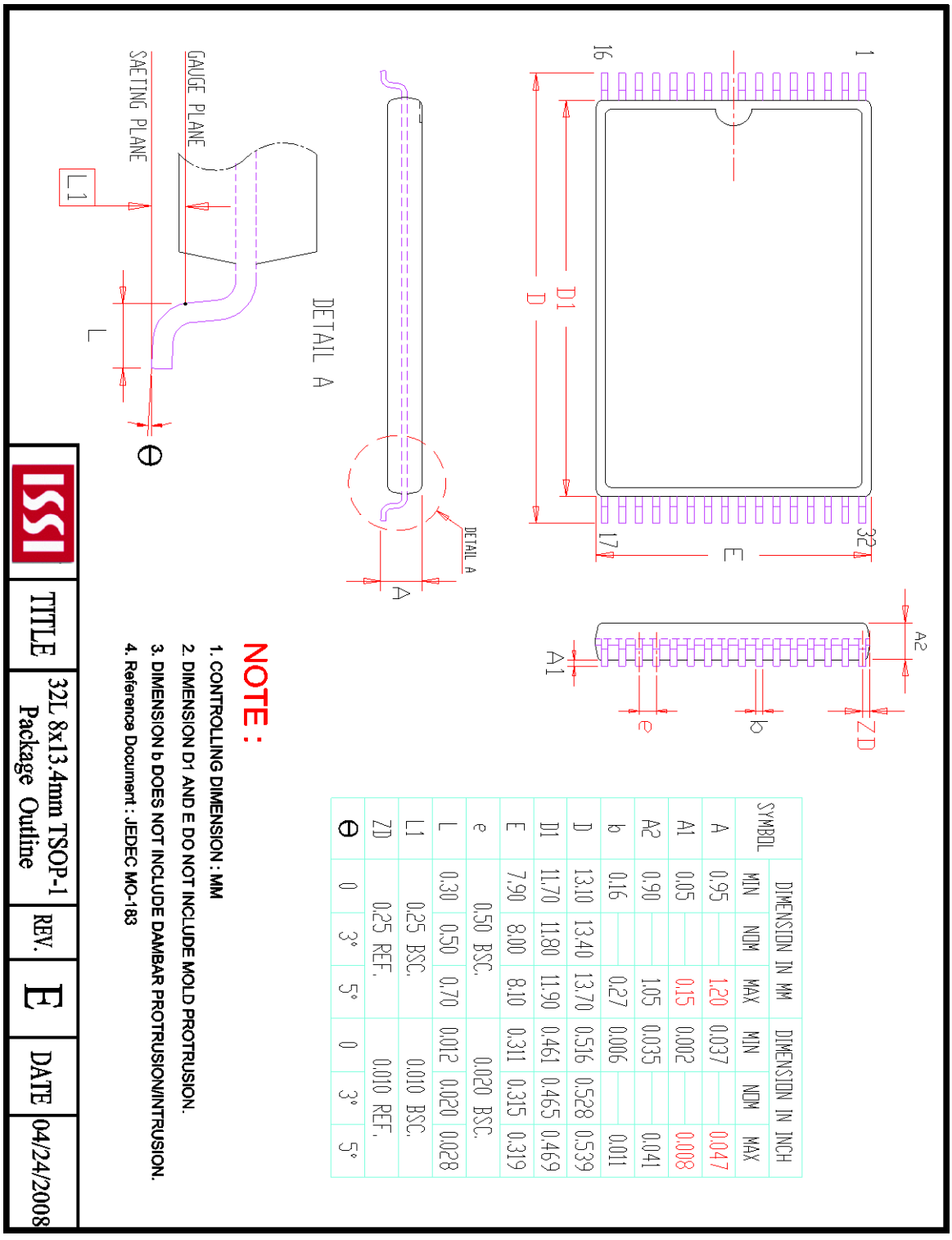
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV5128EHBLL-45TLI	TSOP, Type I (8 x 20 mm), Lead-free
45	IS62WV5128EHBLL-45T2LI	TSOP, Type II, Lead-free
45	IS62WV5128EHBLL-45HLI	sTSOP (Type I), (8 x 13.4 mm), Lead-free
45	IS62WV5128EHBLL-45BI	mini BGA (6mm x 8mm)
45	IS62WV5128EHBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
45	IS62WV5128EHBLL-45B2I	mini BGA (6mm x 8mm), ERR1/2
45	IS62WV5128EHBLL-45B2LI	mini BGA (6mm x 8mm), Lead-free, ERR1/2

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV5128EHBLL-55CT2LA3	TSOP (Type II), Lead-free, Copper Lead-frame
55	IS65WV5128EHBLL-55BLA3	mini BGA (6mm x 8mm), Lead-free
55	IS65WV5128EHBLL-55B2LA3	mini BGA (6mm x 8mm), Lead-free, ERR1/2

PACKAGE INFORMATION

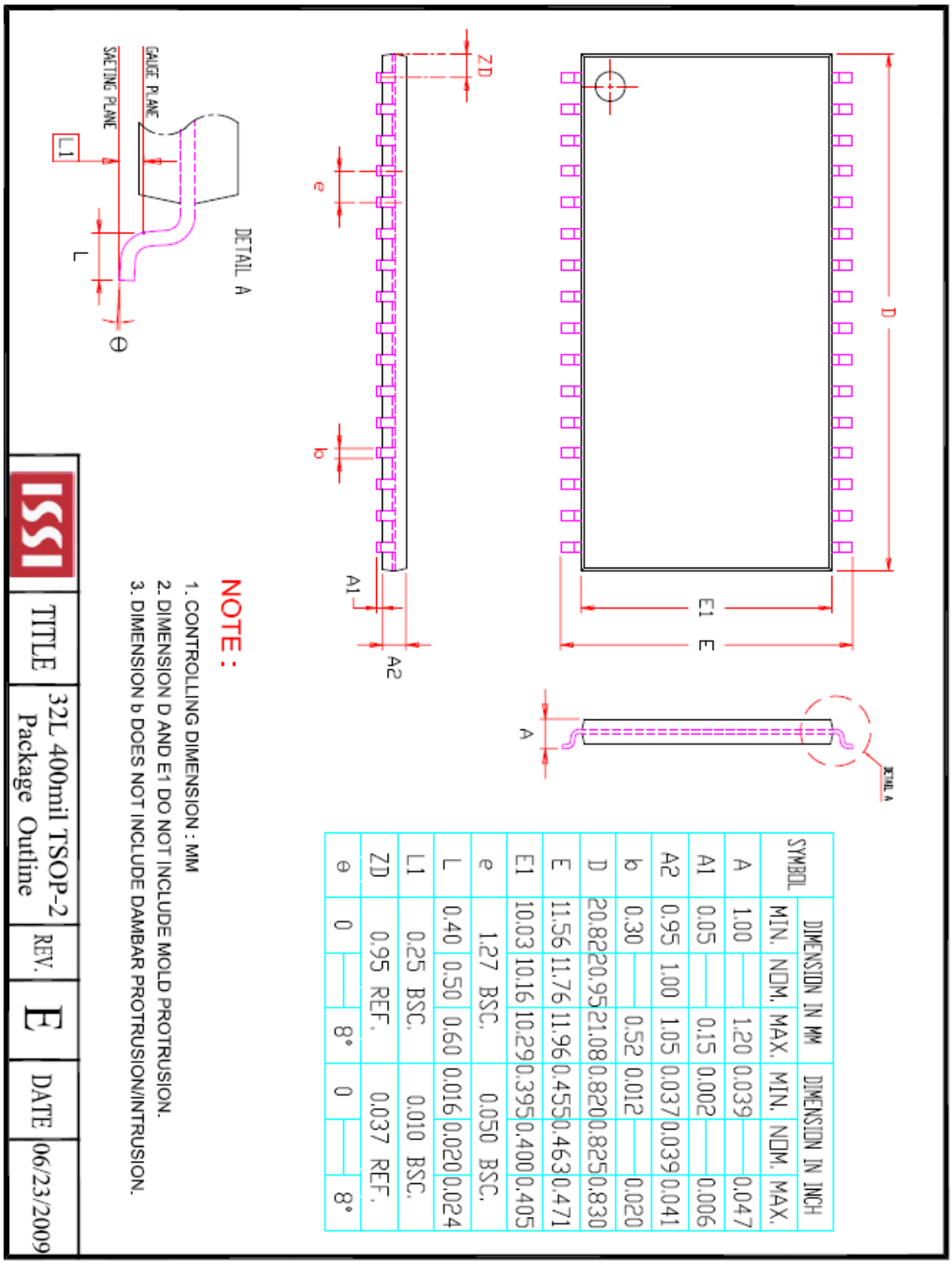


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95	---	1.20	0.037	---	0.047
A1	0.05	---	0.15	0.002	---	0.008
A2	0.90	---	1.05	0.035	---	0.041
b	0.16	---	0.27	0.006	---	0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e		0.50 BSC.			0.020 BSC.	
L	0.30	0.50	0.70	0.012	0.020	0.028
L1		0.25 BSC.			0.010 BSC.	
ZD		0.25 REF.			0.010 REF.	
θ	0	3°	5°	0	3°	5°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	DATE	04/24/2008

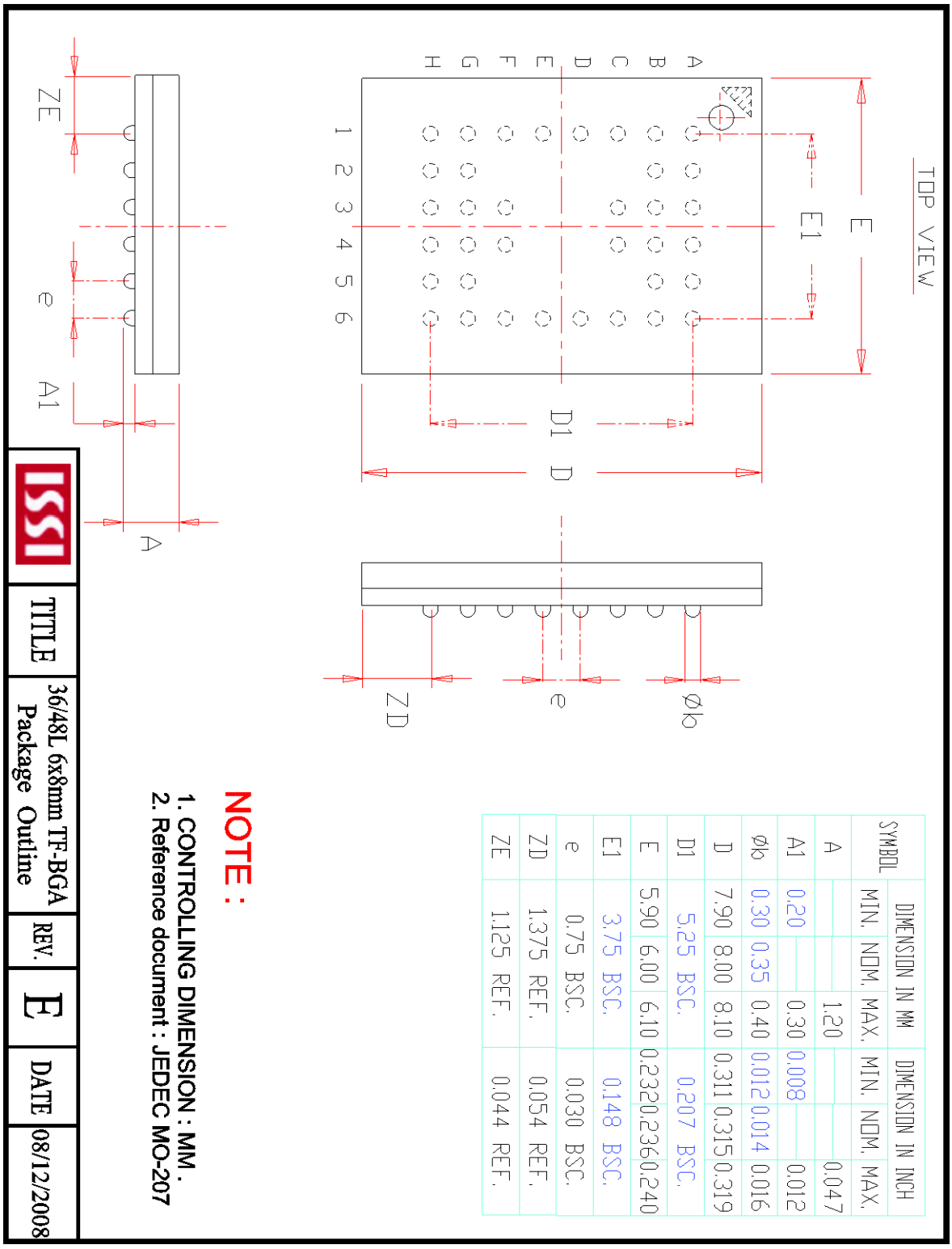


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.52	0.012	—	0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		1.27 BSC.			0.050 BSC.	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.25 BSC.			0.010 BSC.	
ZD		0.95 REF.			0.037 REF.	
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	REV.	DATE	
	32L 400mil TSOP-2 Package Outline	E	06/23/2009	



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20			0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		5.25 BSC.			0.207 BSC.	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		3.75 BSC.			0.148 BSC.	
e		0.75 BSC.			0.030 BSC.	
ZD		1.375 REF.			0.054 REF.	
ZE		1.125 REF.			0.044 REF.	

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

TITLE	36/48L 6x8mm TF-BGA Package Outline
REV.	E
DATE	08/12/2008