IS66WVQ16M4FALL/BLL
IS67WVQ16M4FALL/BLL

64Mb QUADRAM
1.8V/3.0V SERIAL PSRAM MEMORY WITH 200MHZ QUAD DDR (x4 xSPI INTERFACE) PROTOCOL

ADVANCED DATA SHEET

64Mb QUADRAM

SERIAL PSRAM MEMORY WITH 200MHz QUAD DDR (x4 xSPI) Interface

ADVANCED INFORMATION

FEATURES

- **Industry Standard Serial Interface**
  - Quad DDR (x4 xSPI) Interface:
    Command (1 byte) =SDR
    Address (2-byte) & Data = DDR
  - Low Signal Counts :7 Signal pins (CS#, SCLK, DQSM, SIO0~SIO3)

- **High Performance**
  - Double Data Rate (DDR) Operation: 200MHz (200MB/s)
  - Source Synchronous Output signal during Read Operation (DQSM)
  - Data Mask during Write Operation (DQSM)
  - Configurable Latency for Read/Write Operation
  - Supports Variable Latency mode and Fixed Latency mode
  - Configurable Drive Strength
  - Supports Wrapped Burst mode and Continuous Burst mode

- **Burst Operation**
  - Wrapped Burst and Hybrid Wrapped Burst
  - Configurable Wrapped Burst Length: 16B, 32B, 64B, and 128B
  - Byte Order Burst Sequence
  - Continuous Operation:
    Continues Read operation until the end of array address (No Wrapped)
    Continues Write operation even after the end of array address (Wrapped to the first address)

- **Reset Operation**
  - Hardware Reset: RESET# ball.
  - In-Band Reset

- **Supply Voltage**
  - Single 1.7V to 1.95V Voltage Supply
  - Single 2.7V to 3.6V Voltage Supply

- **Hardware Features**
  - **SCLK Input**: Serial clock input
  - **SIO0 – SIO3**:
    Serial Data Input or Serial Data Output
  - **DQSM**:
    - Output during command, address transactions as Refresh Collision Indicator
    - Output during read data transactions as Read Data Strobe
    - Input during write data transactions as Write Data Mask (SDR, Byte Mask)
  - **RESET#:** Hardware Reset pin

- **Low Power Features**
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor.
  - Partial Refresh during Standby mode
  - Supports Deep Power Down mode
  - Ultra Low Power Hybrid Sleep mode with data retained.

- **Temperature Grades**
  - Industrial: -40°C to +85°C
  - Auto (A2) Grade: -40°C to +105°C

- **Industry Standard PACKAGE**
  - B = 24-ball TFBGA 6x8mm 5x5 Array
  - KGD (Call Factory)

GENERAL DESCRIPTION

The IS66/67WVQ16M4FALL/BLL are integrated memory device containing 64Mb Pseudo Static Random Access Memory, using a self-refresh DRAM array organized as 16M words by 4 bits.

The device supports Quad DDR interface, which is compatible with JEDEC standard x4 xSPI Flash.

The device supports Very Low Signal Count (7 signal pins; SCLK, CS#, DQSM, and 4 SIOs), Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Due to DDR operation, minimum transferred data size is a byte (8 bits) through 4 SIO pins.

PERFORMANCE SUMMARY

Read / Write Operation	
Maximum Clock Rate at 3.0V VCC/VCCQ	200MHz
Maximum Clock Rate at 1.8V VCC/VCCQ	200MHz

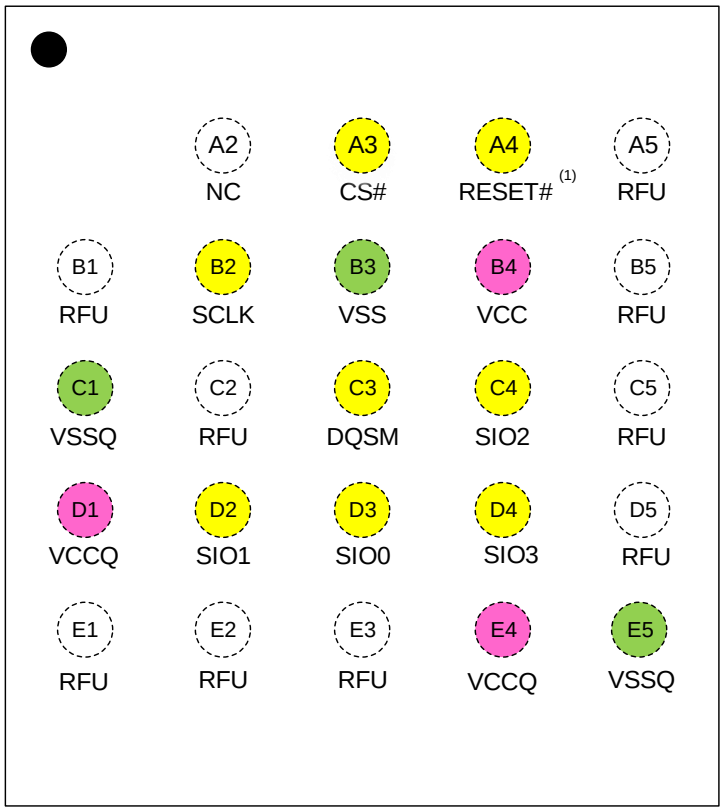
Maximum Current Consumption		
VCC Active Read Current		20 mA
VCC Active Write Current		20 mA
Standby (CS# = High, Full Array)	85°C	200 uA
	105°C	250 uA
Hybrid Sleep (CS# = High, Full Array)	85°C	180 uA
	105°C	200 uA
Deep Power Down (CS# = High)	1.8V, 85°C	20 uA
	3.0V, 85°C	30 uA
	1.8V, 105°C	30 uA
	3.0V, 105°C	50 uA

TABLE OF CONTENTS

1. PIN CONFIGURATION

24-ball TFBGA (5x5 ball array)

Top View, Balls Facing Down



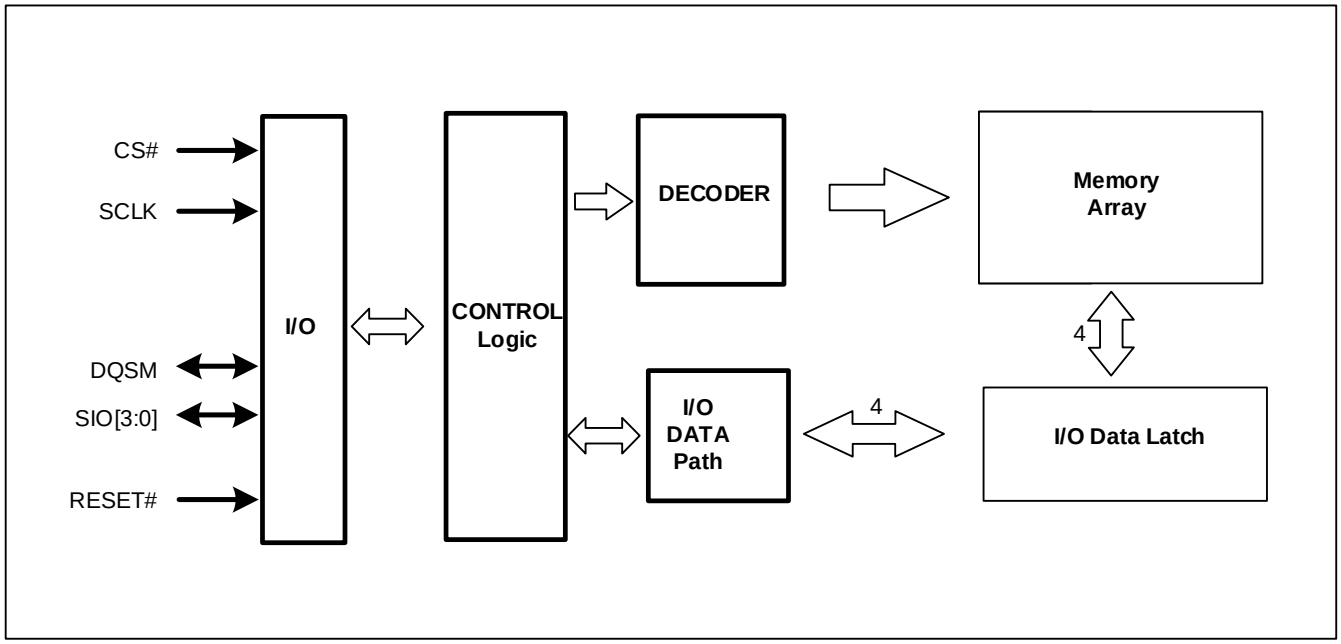
2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CS#	INPUT	**Chip Select:**
DQSM	INPUT/OUTPUT	**Refresh Collision Indicator [2], Data Strobe Signal in Read operation, and Write Data Mask in Write operation:**
RESET#[1]	INPUT	**RESET#:** The RESET# pin is a hardware RESET signal. When RESET# is driven High, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z.
SIO0-SIO3	INPUT	**Serial Data Input & Output pins**.
SCLK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
VCC	POWER	**Power Supply**
VCCQ	POWER	**IO Power Supply**
VSS	GROUND	**Ground**
VSSQ	GROUND	**IO Ground**
RFU	Reserved	**RFU:** Reserved for future use: May or may not be connected internally.

Notes:

1. RESET# pin has an internal pull-up.

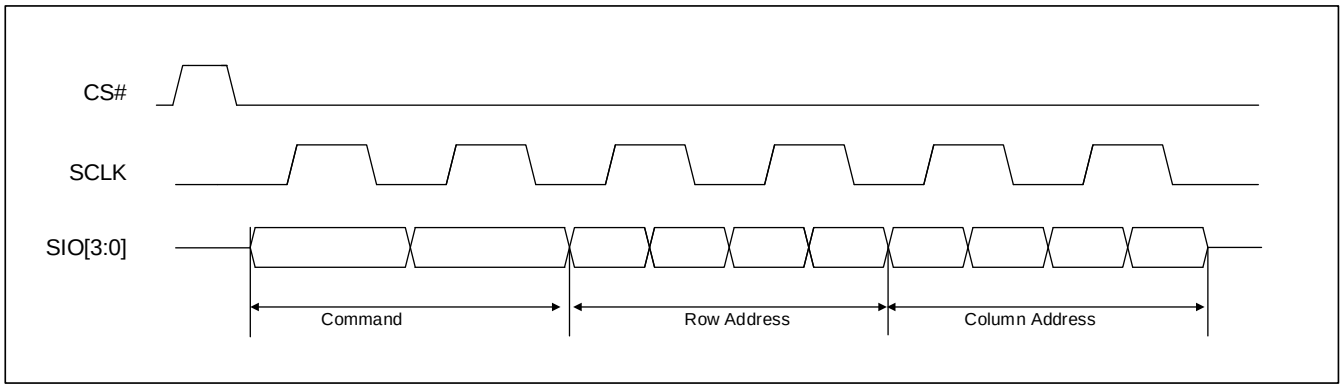
3. BLOCK DIAGRAM



4. COMMAND AND ADDRESS ASSIGNMENTs

The device is serial interface, so all command and address inputs are transferred through SIO pins.

Figure 4.1 Command and Address Cycles



Notes:
1. The figure shows the initial six clock cycles of input operations.
2. Command and Address information is "center aligned" with the clock during both Read and Write operations.

Table 4.1 Command / Address bit assignment

Clock	1st clock	2nd clock	3rd clock		4th clock		5th clock		6th clock	
Function	**Command (8-bit)**		**Row address**				**Column address**			
SIO[3]	Command		Reserved	RA11	RA7	RA3	Reserved	CA6	CA2	Reserved
SIO[2]			Reserved	RA10	RA6	RA2	CA9	CA5	CA1	Reserved
SIO[1]			Reserved	RA9	RA5	RA1	CA8	CA4	CA0	Reserved
SIO[0]			RA12	RA8	RA4	RA0	CA7	CA3	Reserved	Reserved

Notes:

1. The 64Mb QUADRAM address assignments:
   - Row Address 12 ~ 0: 8K (13 bits), Column Address 9 ~ 0: 1K (10 bits), 64Mb density = 8K X 1K (bytes)
2. Data is always transferred in full byte increment (byte granularity -8 bits-transfer).

Table 4.2 Command / Address bit assignment

Command	Clock 1, 2		Clock 3, 4		Clock 5, 6	
	Command (SDR)		Row address (DDR)		Column address (DDR)	
Memory READ with continuous burst	Ah	0h	RA[12:0]		CA[9:0]	
Memory READ with wrapped burst	8h	0h	RA[12:0]		CA[9:0]	
Memory WRITE with continuous burst	2h	0h	RA[12:0]		CA[9:0]	
Memory WRITE with wrapped burst	0h	0h	RA[12:0]		CA[9:0]	
Identification Register (read only)	Ch or Eh	0h	00h	00h	00h	00h
Configuration Register READ	Ch or Eh	0h	00h	04h	00h	00h
Configuration Register WRITE	4h or 6h	0h	00h	04h	00h	00h
Hybrid Sleep Entry (2)	4h or 6h	X	00h	04h	00h	06h

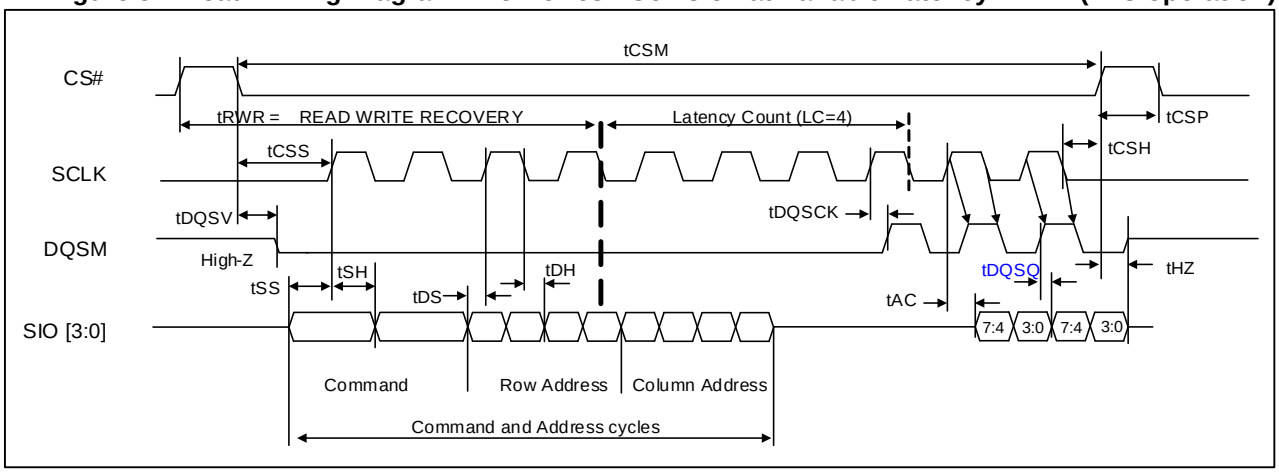
Notes:

1. X = don't care
2. D0 data must be F0h at the rising and falling edge of 7th clock, and CS# must be kept LOW for 8 cycles.

5. Memory READ/WRITE OPERATIONS

5.1 MEMORY READ OPERATIONS

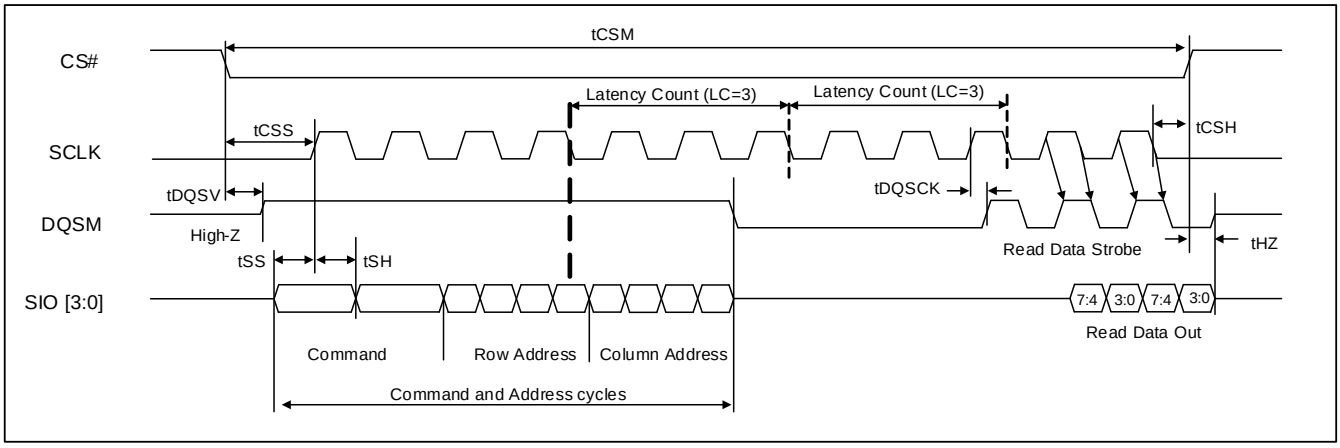
Figure 5.1 Read Timing Diagram - No Refresh Collision at Variable Latency READ (1LC operation)



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with no refresh collision access.**
4. Read access (LC) starts once RA [3:0] (falling edge of 4th clock) is captured.
5. The memory drives DQSM during read cycles.
6. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.

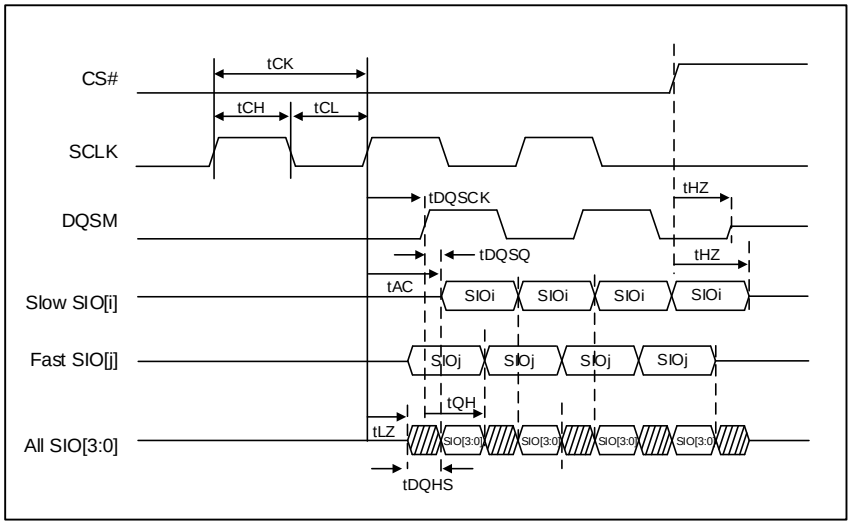
Figure 5.2 Read Timing Diagram - Refresh Collision at Variable-Latency READ (2LC operation)



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access** (2LC operation).
4. In this Read there is a 2 Latency Count (2LC) for read access.
5. Read access (LC) starts once RA [3:0] is captured.
6. The memory drives DQSM during read cycles.
7. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.
8. **Fixed initial READ access latency outputs the first data at a consistent time regardless of worst-case refresh collisions.**

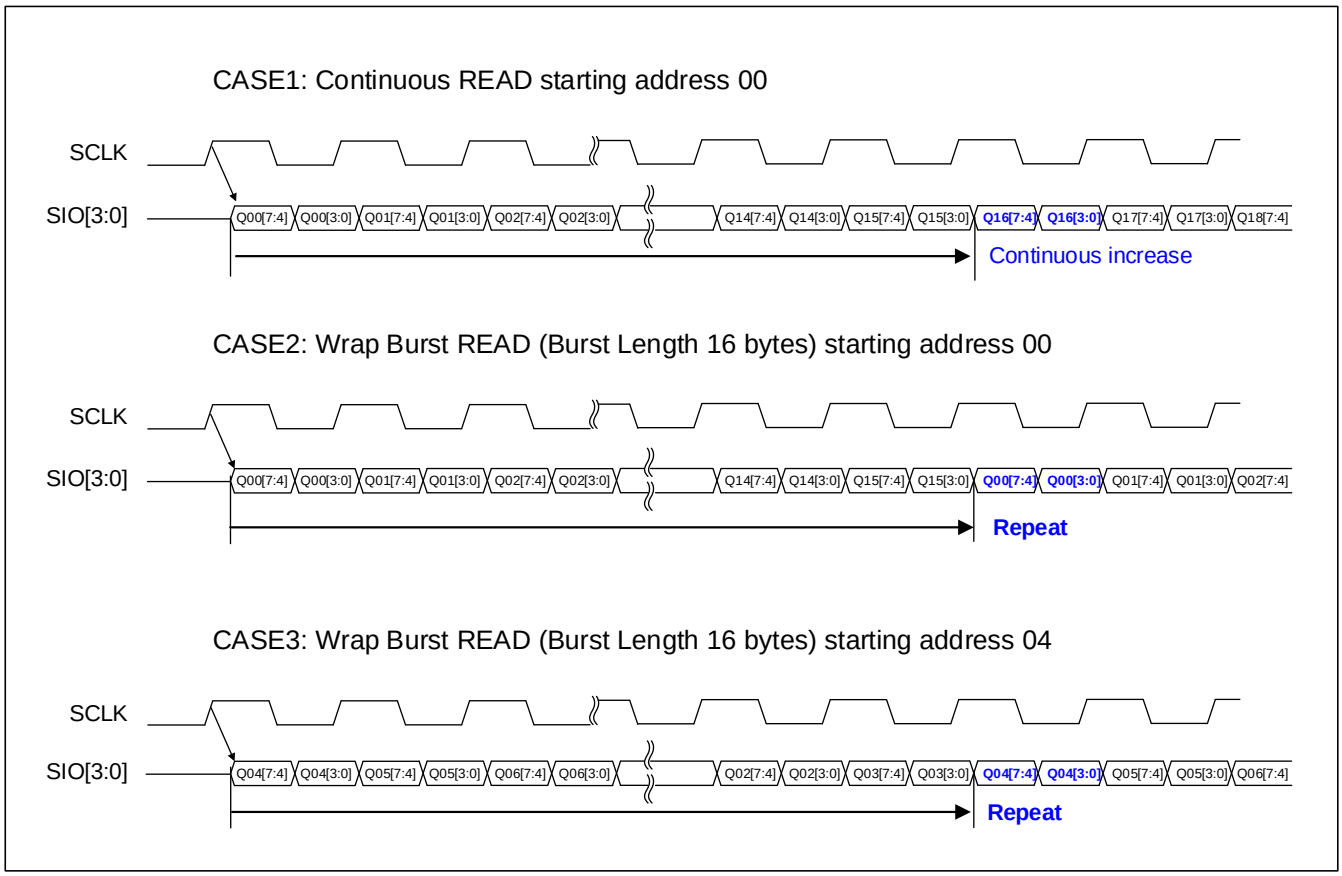
Figure 5.3 Data Valid Timing



Notes:

1. Burst READ data valid timing in detail.
2. tAC defines CLK transition to DQ Valid.
3. tDQSCK defines CLK transition to DQSM Valid.
4. tDQSQ defines DQSM-DQ skew.
5. tQHS defines Data Hold skew factor.
6. tQH defines DQ hold time from DQSM.

Figure 5.4 READ Burst Wrap

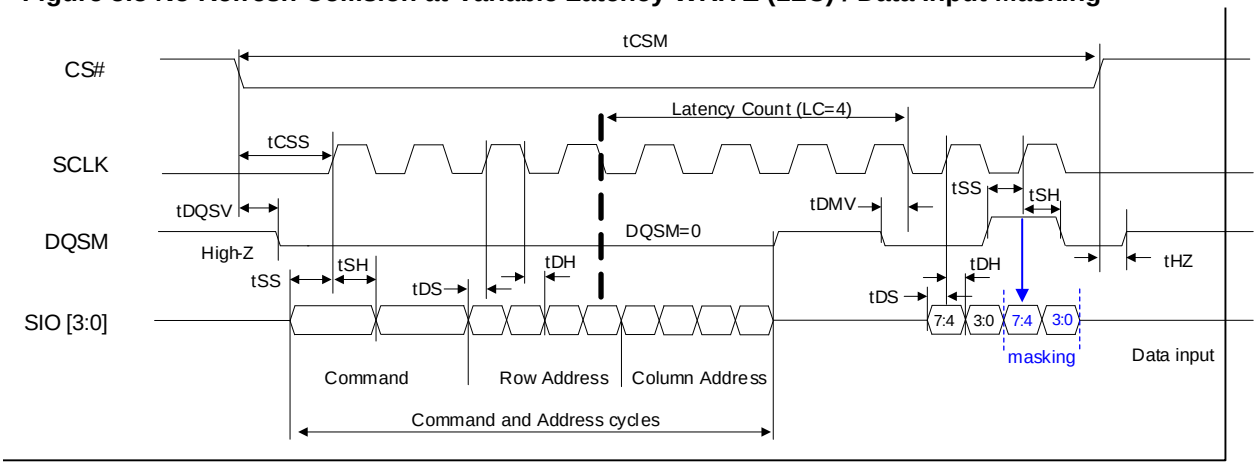


Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Read operation can be ended at any time by bringing CS# High.
3. Continues Read operation until last address. Continuing beyond last address, undefined data will be available.

5.2 WRITE OPERATIONS

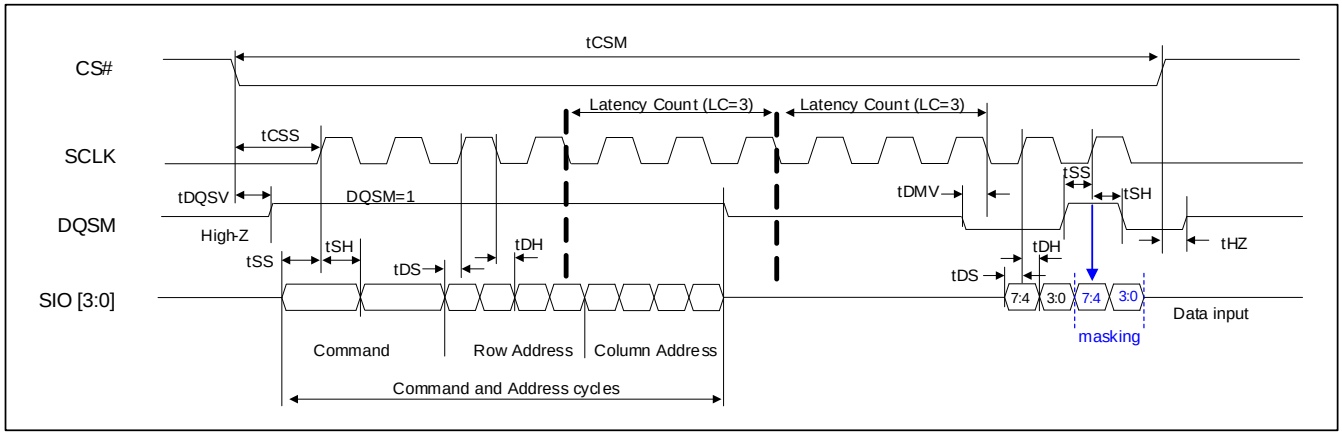
Figure 5.5 No Refresh Collision at Variable Latency WRITE (1LC) / Data Input Masking



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks.
3. Diagram in the figure above is representative of **variable latency with no refresh collision access.**
4. Write access (LC) starts once RA [3:0] is captured.
5. The memory drives DQSM "Low" during command address cycles and DQSM goes to "Hi-Z" after command address cycles.
6. The system memory controller must drive DQSM to a valid Low before the end of initial latency (tDMV) to provide a data mask preamble time. This can be done during the last cycle of LC cycle.
7. During Write data input, data is center aligned with the clock.
8. During Write data input, DQSM indicates whether each data byte is masked with DQSM High or not masked with DQSM Low. **DQSM is SDR for data input masking, and is sampled at the rising edge of clock only**, and will mask whole 8 bits when DQSM is High at the rising edge of clock.
9. Data inputs [7:4] and [3:0] are masked.

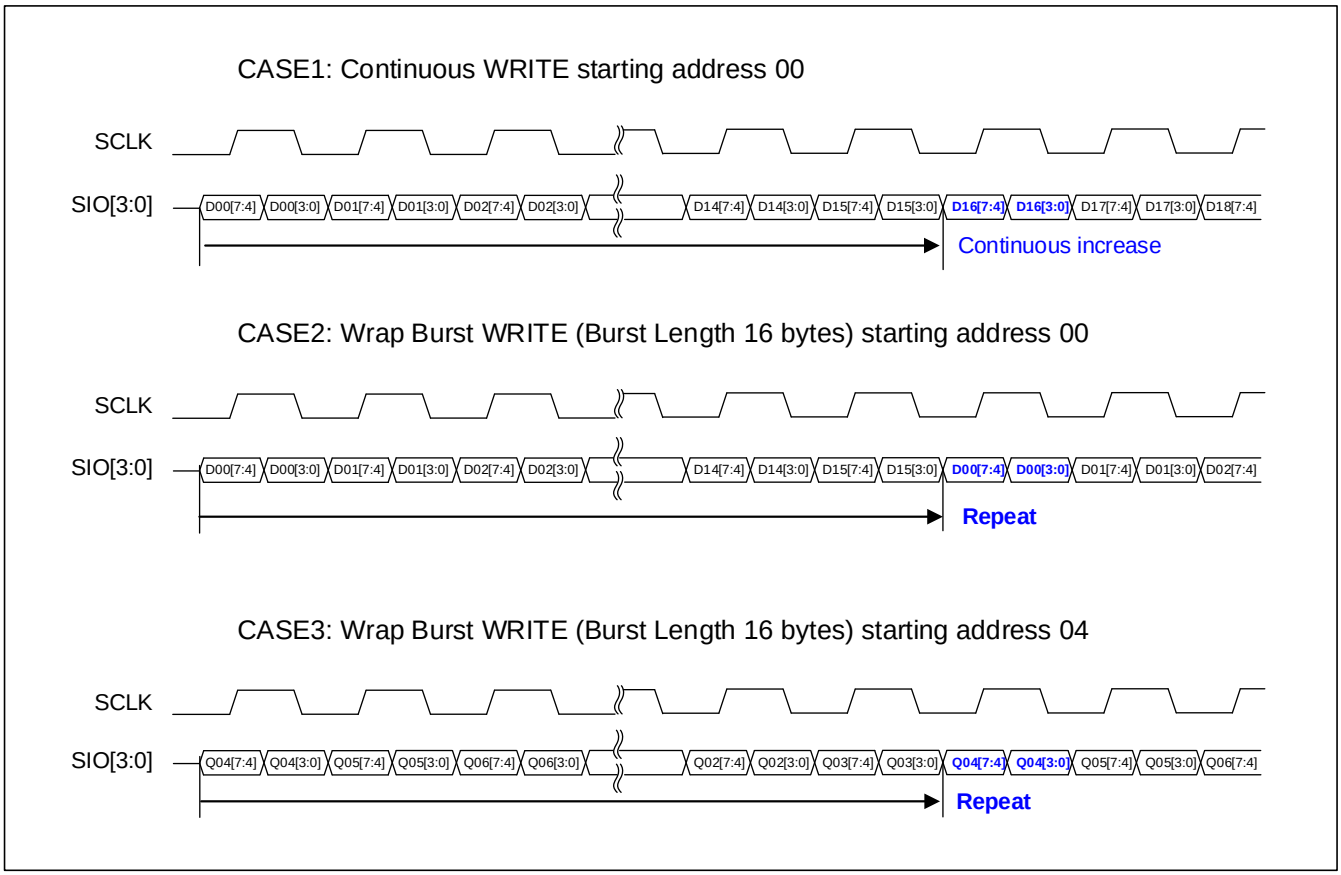
Figure 5.6 Refresh Collision at Variable Latency WRITE (2LC) / Data Input Masking



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks.
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access. (2LC operation)**
4. **In this Write there is a latency count (2LC) for WRITE operation**
5. Write access (LC) starts once RA [3:0] is captured.
6. The memory drives DQSM High during command address cycles and DQSM goes to “Hi-Z” after command address cycles.
7. The system memory controller must drive DQSM to a valid Low before the end of initial latency (tDMV) to provide a data mask preamble time. This can be done during the last cycle of LC cycle.
8. During Write data input, data is center aligned with the clock.
9. During Write data input, DQSM indicates whether each byte (8-bit) is masked with DQSM High or not masked with DQSM Low. **DQSM is SDR for data input masking, and is sampled at the rising edge of clock only**, and will mask whole 8 bits when DQSM is High at the rising edge of clock.
10. Data inputs [7:4] and [3:0] are masked.

Figure 5.7 WRITE Burst Wrap



Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Write operation can be ended at any time by bringing CS# High.
3. When continuous burst write reaches the last address in the memory array, continuing the burst will write to the beginning of the address.

5.3 RESET OPERATION

5.3.1 Hardware RESET Operation

Figure 5.8 RESET# Timing

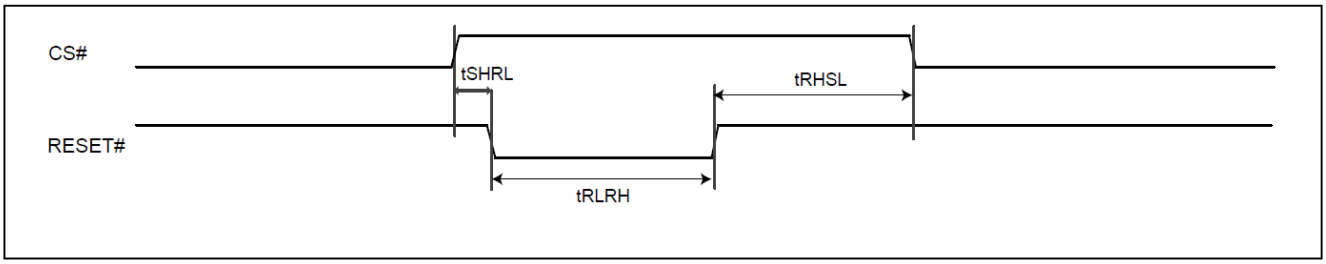


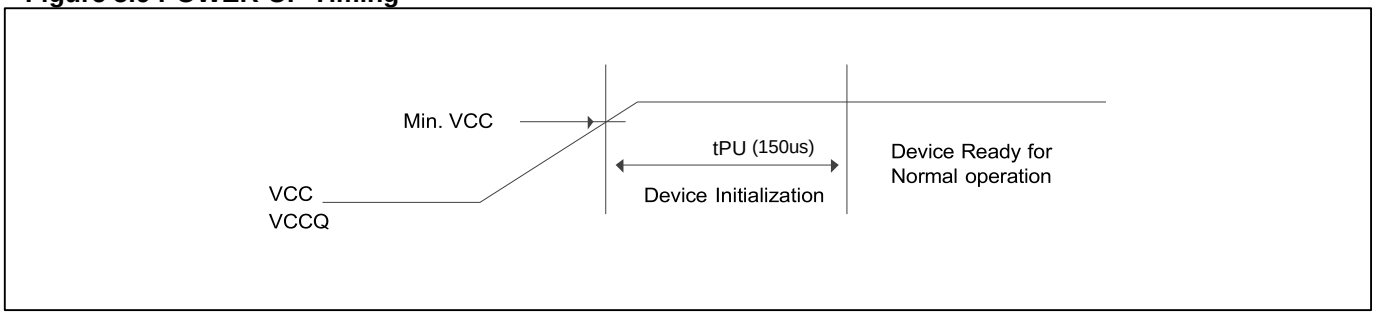
Table 5.1 RESET# Timing Parameters

Parameter	Description	Min	Max	Unit
tSHRL	RESET# Low after CS# High	15	-	ns
tRLRH	RESET# Low Pulse width	10	-	us
tRHSL	RESET# High before CS# Low	10	-	us

5.4 POWER -UP INITIALIZATION

The device includes an on chip voltage sensor used to start device initialization process when VCC, VCCQ reaches Min. VCC. It will require 150us to complete Power On Device Initialization process. After tPU of 150us from min. VCC, the device is ready for Normal operation.

Figure 5.9 POWER-UP Timing

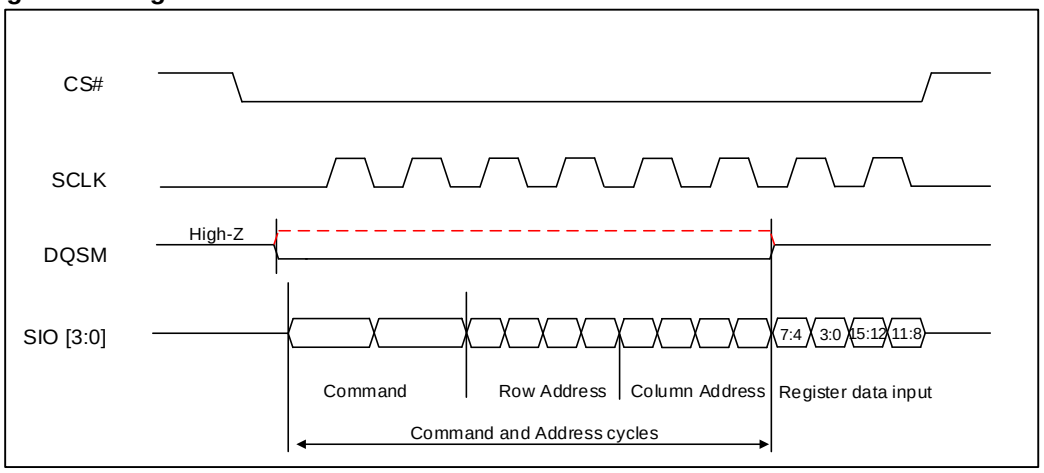


6. REGISTER

The device has 16 bit Configuration Register and ID Register, and they can be accessed by Register Read or Write command.

6.1 REGISTER READ/WRITE OPERATION

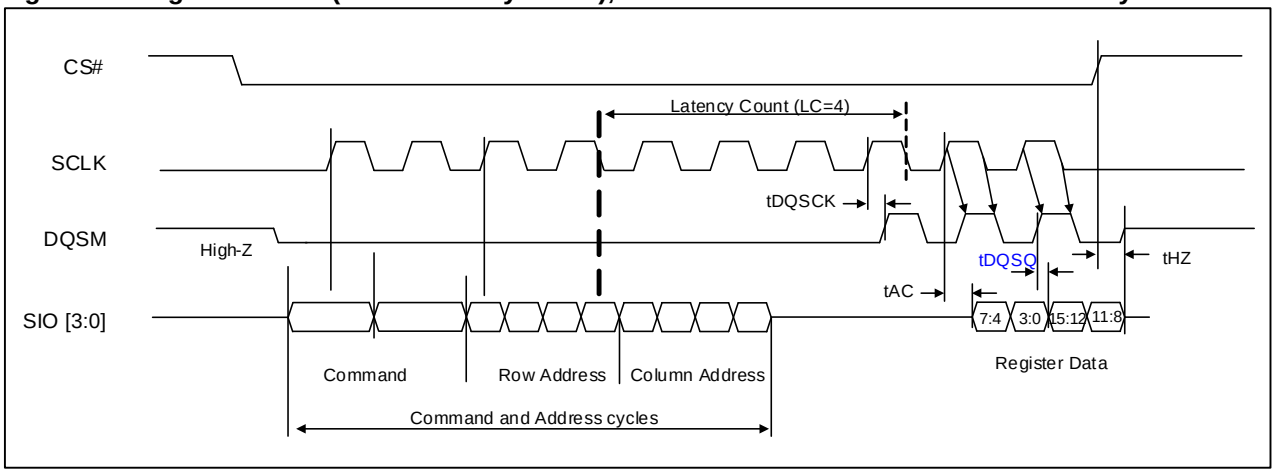
Figure 6.1 Register WRITE



Notes:

1. The device drives DQSM "Low or High for Refresh indication" during command address cycles, which must be ignored by host. DQSM goes to "Hi-Z" after command address cycles.
2. The register value is always provided immediately after the Command Address cycles (0 cycle latency)
3. The DQSM signal keep Hi-Z during register data-input cycles. DQSM will be ignored by host during entire register write operation.
4. **Least Significant Byte first ([7:0]), and Most Significant Byte ([15:8]) later.**

Figure 6.2 Register READ (Initial Latency = 1LC), No Refresh Collision at Variable Latency



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with no refresh collision access.**
4. Read access (LC) starts once RA [3:0] is captured (falling edge of 4th Row address clock)
5. The memory drives DQSM during read cycles.
6. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.

6.2 CONFIGURATION REGISTER

The Configuration Register is able to change the defaulted status of the device. The device will be configured after the CR bit is set.

Table 6.1 Configuration Register

Bit	Function	Settings (Binary)
15	Deep Power Down Enable	1- Normal operation (default) 0- Writing 0 to CR [15] causes the device to enter Deep Power Down.
14-12	ODS (Output Drive Strength)	Refer to *"Table 6.2. Output Driver Strength Table"*
11-9	Partial Array Refresh	**000- Full Array (default)** 001- Bottom 1/2 Array 010- Bottom 1/4 Array 011- Bottom 1/8 Array 100- Reserved 101- Top 1/2 Array 110- Top 1/4 Array 111- Bottom 1/8 Array
8	**DQSM READ Pre-cycle**	**1 - 1 clock** **0 - 0 clock (default)**
7-4	Latency count	Refer to *"Table 6.3. Latency count Table"*
3	Initial Access Latency	**0 - Variable Latency (default)** 1 - Fixed Latency
2	Burst Type	**0 - Wrapped (default)** 1 – Hybrid Wrapped
1-0	Burst Length	00- 128 bytes 01- 64 bytes **10- 32 bytes (default)** 11- 16 bytes

Table 6.2 Output Driver Strength Table

CR[14]	CR[13]	CR[12]	Description
0	0	0	100 Ohms
0	0	1	66 Ohms
0	1	0	50 Ohms
0	1	1	40 Ohms
1	0	0	33 Ohms
1	0	1	33 Ohms
1	1	0	25 Ohms
1	**1**	**1**	**25 Ohms (Default)**

Table 6.3 Latency Count Table

CR[7:4]	Latency Count
0000	3 clocks
0001	4 clocks
0010	5 clocks
0011	6 clocks
0100	**7 clocks (default)**
0101	8 clocks
0110~1111	Reserved

6.2.1 WRAPPED BURST LENGTH

32 Byte Wrap is the default setting after power on. If Hybrid Burst Wrap is selected, the device will burst through the initial wrapped burst length once, then continues to advance incrementally up to maximum column address (1K) before wrapping around within the entire column address space.

Table 6.4 Wrapped Burst Sequences

Configuration Register[2]	Configuration Register[1:0]	Burst Length	Wrap Boundary Col. Addr	Start Address	Byte Sequence
0	00	Wrap 128	CA[6:0]	4	[4, 5, 6…127, 0, 1, 2, …]
0	01	Wrap 64	CA[5:0]	4	[4, 5, 6…63, 0, 1, 2, …]
0	**10**	**Wrap 32**	**CA[4:0]**	4	[4, 5, 6…31, 0, 1, 2, …]
0	11	Wrap 16	CA[3:0]	4	[4, 5, 6…15, 0, 1, 2, …]
1	00	Hybrid Wrap 128	CA[6:0]	4	[4, 5, 6…127, 0, 1, 2, 3], 128, 129…1023,0,1, …
1	01	Hybrid Wrap 64	CA[5:0]	4	[4, 5, 6…63, 0, 1, 2, 3], 64, 65, 66…1023,0,1, …
1	10	Hybrid Wrap 32	CA[4:0]	4	[4, 5, 6…31, 0, 1, 2, 3], 32, 33, 34…1023,0,1, …
1	11	Hybrid Wrap 16	CA[3:0]	4	[4, 5, 6…15, 0, 1, 2, 3], 16, 17, 18…1023,0,1, …
X	XX	Continuous	X	4	4, 5, 6, 7…1023, 1024, 1025…2043, 2044, 2045, …

When Continuous burst command is inserted, memory access address will increase continuously up to entire memory array regardless of Burst Type setting and Burst Length setting until CS# is going to HIGH.

When a continuous burst read reaches the last address of the memory array, continuing the burst beyond the last address will provide undefined data.

When a continuous burst write reaches the last address of the memory array, continuing the burst beyond the last address will write to the beginning of the address range

6.2.2 INITIAL LATENCY (CR [3])

Initial Latency for Variable Latency setting (CR [3]=0) is LC or 2LC , based on Refresh Collision like below table. So host chipset must monitor DQSM signal, which indicates Refresh Collision occurrence or not.
But Initial Latency for Fixed Latency setting (CR [3] = 1) is always 2LC.

Table 6.5 Variable Latency (CR[3] = 0)

Latency code CR[7:4]	Initial Latency Count		Maximum Operating Frequency	
	No Refresh Collision (LC)	Refresh Collision (2LC)	1.8V	3.0V
0000	3 clocks	6 clocks	83Mhz	83Mhz
0001	4 clocks	8 clocks	100Mhz	100Mhz
0010	5 clocks	10 clocks	133Mhz	133Mhz
0011	6 clocks	12 clocks	166MHz	166MHz
0100	**7 clocks(default) (1)**	**14 clocks**	**200MHz**	**200MHz**
0101	8 clocks	16 clocks	200Mhz	200MHz
0100 - 1111	Reserved	-	NA	

Note:
1. Contact ISSI MKT for default setting of 1.8V - 8 clocks, and 3.0V – 5 clocks.

Table 6.6 Initial Latency Summary Table(1)

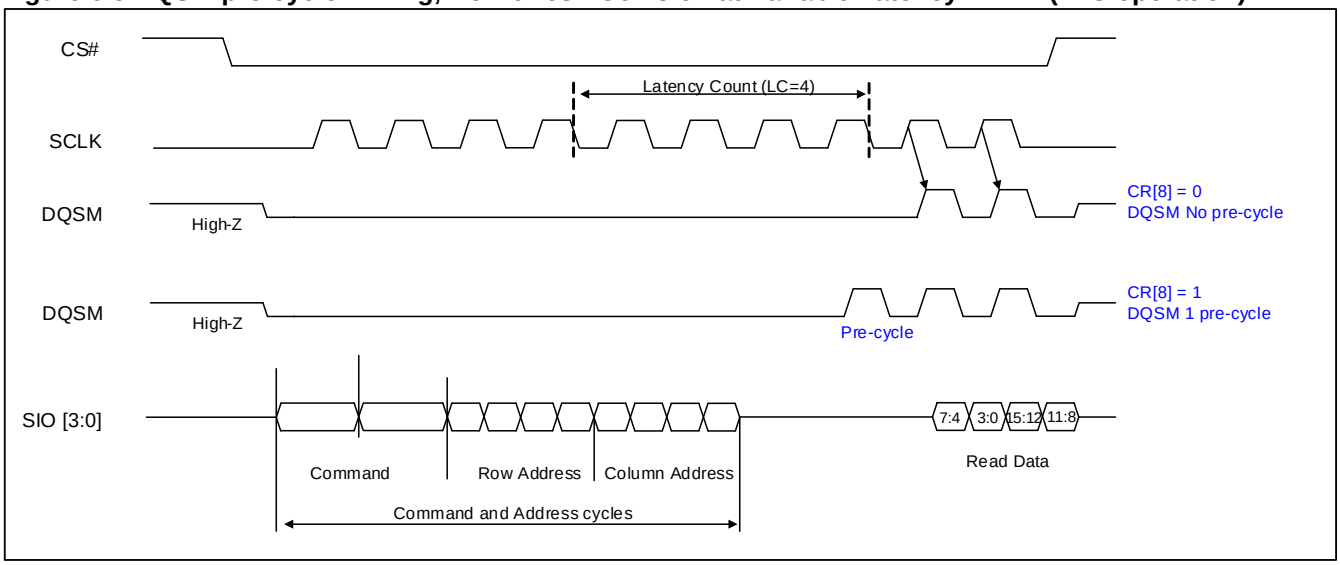
Destination	Operating mode	Variable mode (default) initial Latency Count		Fixed mode Initial Latency Count
		No Refresh Collision	Refresh Collision	
Memory	READ	1LC	2LC	2LC
	WRITE	1LC	2LC	2LC
Register	READ	1LC	2LC	2LC
	WRITE	0LC		0LC

Note:
1. LC means Latency Count clocks, which is in Configuration Register Bit [7:4], as defined in *"Table 6.1" and "Table 6.3"*.

6.2.3 DQSM READ Pre-Cycle (CR [8])

CR [8] defines DQSM Pre-Cycle.

Figure 6.3 DQSM pre-cycle Timing, No Refresh Collision at Variable Latency READ (1LC operation)



Notes:

1. Latency count (LC) is 4 clocks.
2. When Configuration Register bit [8] = 0, the Device will output DQSM with valid data cycle.
3. When Configuration Register bit [8] = 1, the Device will output 1 pre-cycle (dummy DQSM) prior to valid data cycle.
4. The memory drives DQSM during read cycles.

6.2.4 Deep Power Down (CR [15])

Figure 6.4 Deep Power Down Entry Timing

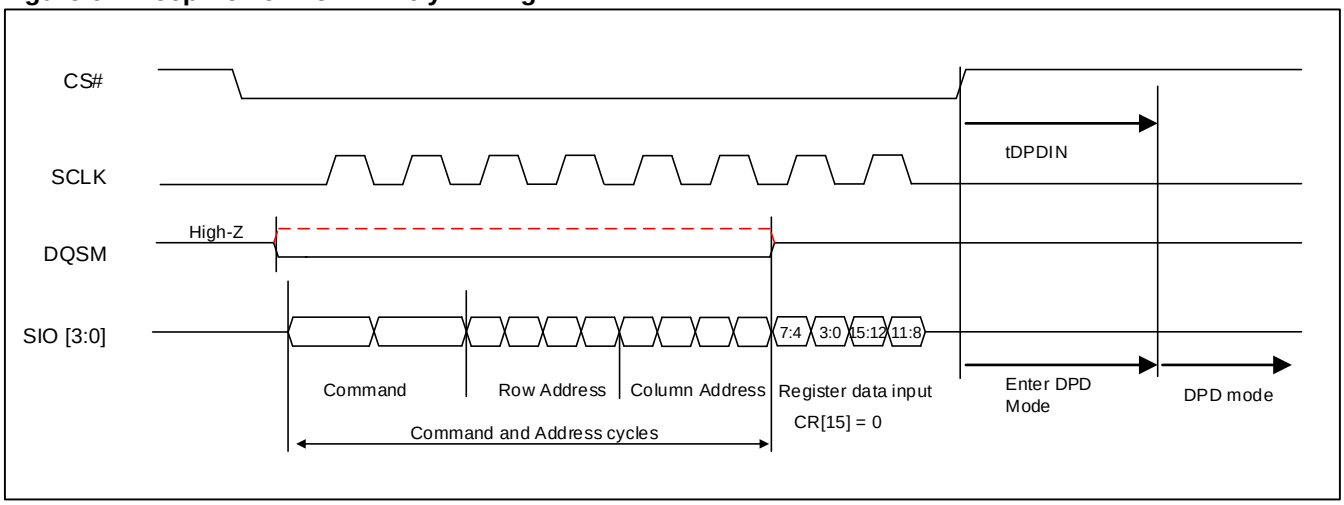
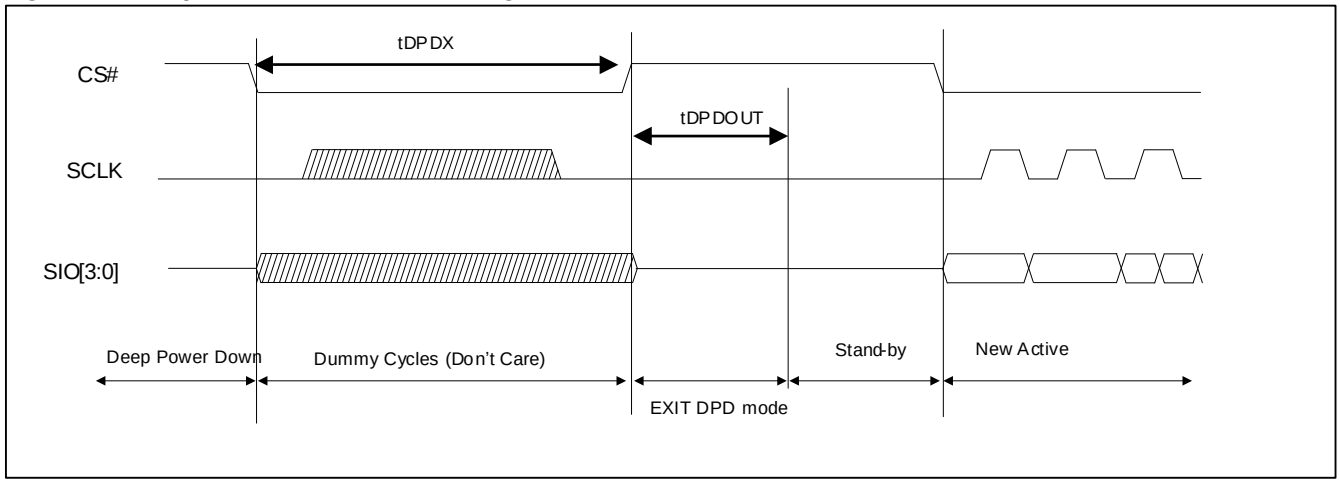


Figure 6.4 Deep Power Down Exit Timing



Note: Memory Cell Data cannot be retained at deep power down(DPD) mode.

Table 6.7 Deep Power Down Timing Parameters

Parameter	Description	Min	Max	Unit
tDPDIN	Deep Power Down CR[15]=0 register write to DPD power level	150	-	us
tDPDX	CS# Low period to exit from Deep Power Down	200	-	ns
tDPDOUT	CS# Low then High to Standby wakeup time	-	150	us

6.2.5 Partial Refresh (CR [11:9])

The partial array refresh configuration restricts the refresh operation in QUADRAM to a portion of the memory array specified by CR [11:9]. This reduces standby current. The default configuration refreshes the whole array.

6.3 DEVICE IDENTIFICATION REGISTER

It is a read only, non-volatile, word register that provides device information The device information fields can be identified as below.

a. Device Type
b. Density
    i. Row address bit count
    ii. Column address bit count
c. Manufacturer

Table 6.8 ID Register

Bits	Function	Settings (Binary)
15 - 13	Device Voltage	000: 1.8V 001: 3V
12 - 8	Row address bit count	00000 : 1 row address ……. 01100 : 13 row address …….. 11111 : 32 row address
7 - 4	Column address bit count	0000 : 1 column address ….. 1001: 10 column address ….. 1111 : 16 column address
3 - 0	Manufacturer	0011 (ISSI)

6.4 IN BAND RESET

The device offers an additional feature of In-Band RESET function, which uses existing SPI signals to initiate a hardware reset, which is different from existing software reset/hardware reset (dedicated RESET# pin);

- Existing software reset commands often depend on the Flash being in a particular mode before they are effective. This makes software based reset sequences depend on slave device and mode.
- Dedicated RESET# pin requires additional pin over traditional 8-pins of SPI device. Also it requires 1 more signal for reset operation.

In Band-RESET operation requires 2-signal pins; CE# and SIO0.

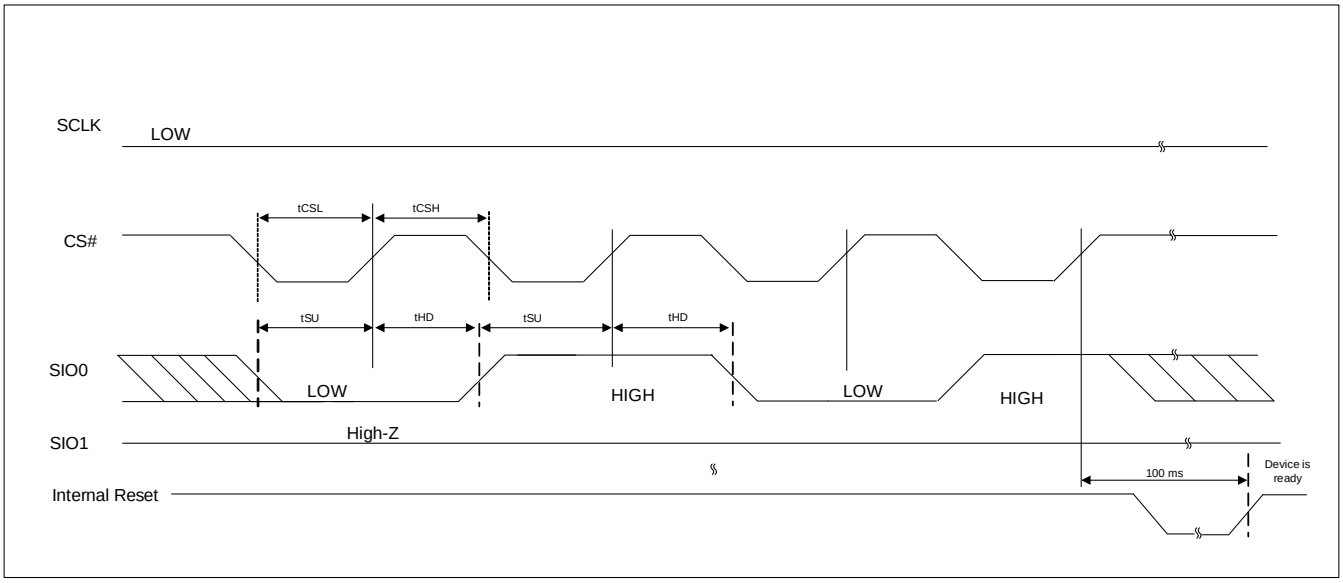
- CS# is driven active low to select the SPI slave (note1)
- Clock (SCLK) remains stable in either a high or low state ….(note 2)
- SIO0 is driven low by the bus master, simultaneously with CS# going active low……(note 3)
- CS# is driven inactive … (note 4)
- Repeat the above 4 steps, each time alternating the state of SIO0.
- After the fourth CS# pulse, the slave triggers its internal reset……..(note 5)

Note 1 This powers up the SPI slave
Note 2 This prevents any confusion with a command, as no command bits are transferred (clocked)
Note 3 No SPI bus slave drives SIO0 during CS# low before a transition of clock. Slave streaming output active is not allowed until after the first edge of clock.
Note 4 The slave captures the state of SIO0 on the rising edge of CS#
Note 5 SIO0 is low on the first CS#, high on the second, low on the third, high on the fourth … (This provides a 5th, unlike random noise)

NOTE:

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. During the reset process, the device will ignore any chip select (command).

Figure 6.5 Timing for In-Band RESET Operation

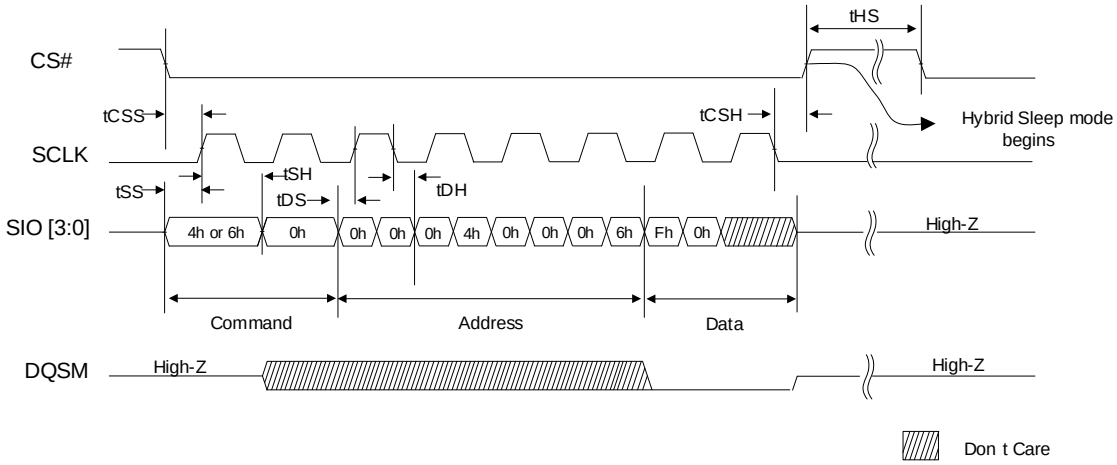


Parameter	Symbol	Min	Max	Units
CS# Low Pulse	tCSL	500	--	ns
CS# High Pulse	tCSH	500	--	ns
Setup Time	tSU	5	--	ns
Hold Time	tHD	5	--	ns

6.5 HYBRID SLEEP MODE

Hybrid Sleep Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Hybrid Sleep Mode Entry is entered when CS# going HIGH after command, address, and data. Hybrid Sleep Mode must be maintained for the minimum duration of tHS. The Hybrid Sleep Mode Entry command sequence is shown like below.

Figure 6.6 Hybrid Sleep Mode Entry Timing Diagram



Hybrid Sleep Mode Exit is initiated by a low pulsed CS# of tCSHS. Afterwards, CS# should be held HIGH of tEXTHS until the first operation begins.

Figure 6.7 Hybrid Sleep Mode Exit Timing Diagram

Table 6.9 Hybrid Sleep Mode Timing Parameter

Parameter	Symbol	Min	Max	Units
Minimum Hybrid Sleep Mode duration	tHS	150	-	us
CS# LOW pulse width to exit from Hybrid Sleep Mode	tCSHS	60	-	ns
CS# LOW then High to device ready time	tEXTHS	70	-	us

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature	-65°C to +150°C
Voltage with Respect to Ground on All Pins	-0.5V to V_{CC} / V_{CCQ} + 0.5V
Voltage on V_{CC} supply relative to Ground	-0.5V to V_{CC} + 0.5V
Voltage on V_{CCQ} supply relative to Ground	-0.5V to V_{CCQ} + 0.5V
Electrostatic Discharge Voltage (Human Body Model)(2)	-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

7.2 OPERATING RANGE

Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Supply Voltage	IS66/67WVQ16M4FALL	1.70V (VMIN) –1.95V (VMAX); 1.8V (Typ)
	IS66/67WVQ16M4FBLL	2.7V (VMIN) –3.6V (VMAX); 3.0V (Typ)
V_{CCQ} I/O Supply Voltage	IS66/67WVQ16M4FALL	1.70V (VMIN) –1.95V (VMAX); 1.8V (Typ)
	IS66/67WVQ16M4FBLL	2.7V (VMIN) –3.6V (VMAX); 3.0V (Typ)

7.3 DC CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Leakage Current Reset Signal High Only		-	-	±1.0	uA	VIN = V_{SSQ} to V_{CCQ}, V_{CCQ} = V_{CCQ} max
I_{LI}(4)	Input Leakage Current Reset Signal Low Only		-	-	±15.0	uA	VIN = V_{SSQ} to V_{CCQ}, V_{CCQ} = V_{CCQ} max
I_{CC1}	V_{CC} Active Read Current		-	15	20	mA	CS# = VIL, @200MHz, V_{CC} = 3.6V
				15	20		CS# = VIL, @200MHz, V_{CC} = 1.95V
I_{CC2}	V_{CC} Active Write Current		-	15	20	mA	CS# = VIL, @200MHz, V_{CC} = 3.6V
				15	20		CS# = VIL, @200MHz, V_{CC} = 1.95V
I_{CC4I}	V_{CC} Standby Current 1.8V for Industrial (-40°C to +85°C)	Full array	-	120	200	uA	CS#, V_{CC} = 1.95V
		Bottom 1/2 array		100	160		
		Bottom 1/4 array		90	130		
		Bottom 1/8 array		80	100		
		Top 1/2 array		100	160		
		Top 1/4 array		90	130		
		Top 1/8 array		80	100		
	VCC Standby Current 3.0V for Industrial (-40°C to +85°C)	Full array	-	150	200		CS#, V_{CC} = 3.6V
		Bottom 1/2 array		120	160		
		Bottom 1/4 array		100	130		
		Bottom 1/8 array		90	100		
		Top 1/2 array		120	160		
		Top 1/4 array		100	130		
		Top 1/8 array		90	100		
I_{CC4IP}	V_{CC} Standby Current 1.8V for Extended (-40°C to +105°C)	Full array		120	250		CS#, V_{CC} = 1.95V
		Bottom 1/2 array		100	210		
		Bottom 1/4 array		90	180		
		Bottom 1/8 array		80	150		
		Top 1/2 array		100	210		
		Top 1/4 array		90	180		
		Top 1/8 array		80	150		
	VCC Standby Current 3.0V for Extended (-40°C to +105°C)	Full array		150	250		CS#, V_{CC} = 3.6V
		Bottom 1/2 array		120	210		
		Bottom 1/4 array		100	180		
		Bottom 1/8 array		90	150		
		Top 1/2 array		120	210		
		Top 1/4 array		100	180		
		Top 1/8 array		90	150		
I_{CC5}	Reset Current		-	-	1	mA	CS# = VIH, RESET# = V_{ss} +/- 0.3V, V_{CC} = V_{CC} max
I_{CC6I}	Active Clock Stop Current for Industrial (-40°C to +85°C)		-	5	8	mA	CS# = VIL, RESET# = V_{CC} +/- 0.3V, V_{CC} = VCC max
I_{CC6IP}	Active Clock Stop Current for Extended (-40°C to +105°C)		-	5	12		
I_{CC7}	V_{CC} Current during power up		-	-	35	mA	CS#= H, V_{CC}= V_{CC} max, V_{CC}=V_{CCQ}= 1.95V or 3.6V
I_{DPDI}	Deep Power Down Current 1.8V for Industrial (-40°C to +85°C)		-	-	20	uA	CS#, V_{CC} = 1.95V
	Deep Power Down Current 3.0V for Industrial (-40°C to +85°C)		-	-	30		CS#, V_{CC} = 3.6V
I_{DPDIP}	Deep Power Down Current 1.8V for Extended (-40°C to +105°C)		-	-	30		CS#, V_{CC} = 1.95V
	Deep Power Down Current 3.0V for Extended (-40°C to +105°C)		-	-	50		CS#, V_{CC} = 3.6V

Symbol	Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_{HSI}	Hybrid Sleep Current 1.8V for Industrial (-40°C to +85°C)	Full array	-	100	180	uA	CS#, V_{CC} = 1.95V
		Bottom 1/2 array		80	150		
		Bottom 1/4 array		70	120		
		Bottom 1/8 array		60	90		
		Top 1/2 array		80	150		
		Top 1/4 array		70	120		
		Top 1/8 array		60	90		
	Hybrid Sleep Current 3.0V for Industrial (-40°C to +85°C)	Full array	-	120	180		CS#, V_{CC} = 3.6V
		Bottom 1/2 array		100	150		
		Bottom 1/4 array		90	120		
		Bottom 1/8 array		80	90		
		Top 1/2 array		100	150		
		Top 1/4 array		90	120		
		Top 1/8 array		80	90		
I_{HSIP}	Hybrid Sleep Current 1.8V for Extended (-40°C to +105°C)	Full array		100	200		CS#, V_{CC} = 1.95V
		Bottom 1/2 array		80	170		
		Bottom 1/4 array		70	150		
		Bottom 1/8 array		60	120		
		Top 1/2 array		80	170		
		Top 1/4 array		70	150		
		Top 1/8 array		60	120		
	Hybrid Sleep Current 3.0V for Extended (-40°C to +105°C)	Full array		120	200		CS#, V_{CC} = 3.6V
		Bottom 1/2 array		100	170		
		Bottom 1/4 array		90	150		
		Bottom 1/8 array		80	120		
		Top 1/2 array		100	170		
		Top 1/4 array		90	150		
		Top 1/8 array		80	120		
V_{IL}[2]	Input Low Voltage		-0.5	-	$0.3V_{CCQ}$	V	
V_{IH}[1]	Input High Voltage		$0.7V_{CCQ}$	-	V_{CCQ} + 0.3	V	
V_{OL}	Output Low Voltage			-	0.2	V	I_{OL} = 100 µA
V_{OH}	Output High Voltage		V_{CCQ} - 0.2	-		V	I_{OH} = -100 µA

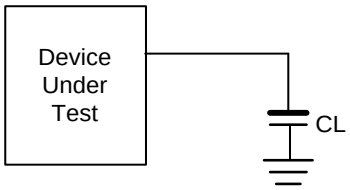
Notes:

1. **Input signals may overshoot V_{CCQ} + 1.0V for periods less than 2ns during transitions.**
2. **Input signals may undershoot V_{SSQ} - 1.0V for periods less than 2ns during transitions.**
3. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ).**
4. **RESET# Low initiates exits from DPD state and initiates the draw of ICC5 reset current, making ILI during Reset# Low insignificant.**

7.4 AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Output Load Capacitance		20	pF
TR,TF	Input Rise and Fall Times	2		V/ns
VIN	Input Pulse Voltages	0V to V_{CCQ}		V
VREFI	Input Timing Reference Voltages	VCCQ/2		V
VREFO	Output Timing Reference Voltages	VCCQ/2		V

Figure 7.1 Test Setup



7.5 PIN CAPACITANCE (TA = 25°C, VCC=1.8V/ 3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance (CS#, SCLK)	V_{IN} = 0V	3	-	4.5	pF
$C_{IN/OUT}$	Input/Output Capacitance (SIO, DQSM)	$V_{IN/OUT}$ = 0V	3	-	4.0	pF

Note:
1. These parameters are characterized and not 100% tested.

7.6 AC CHARACTERISTICS

7.6.1 Read Timing Parameters

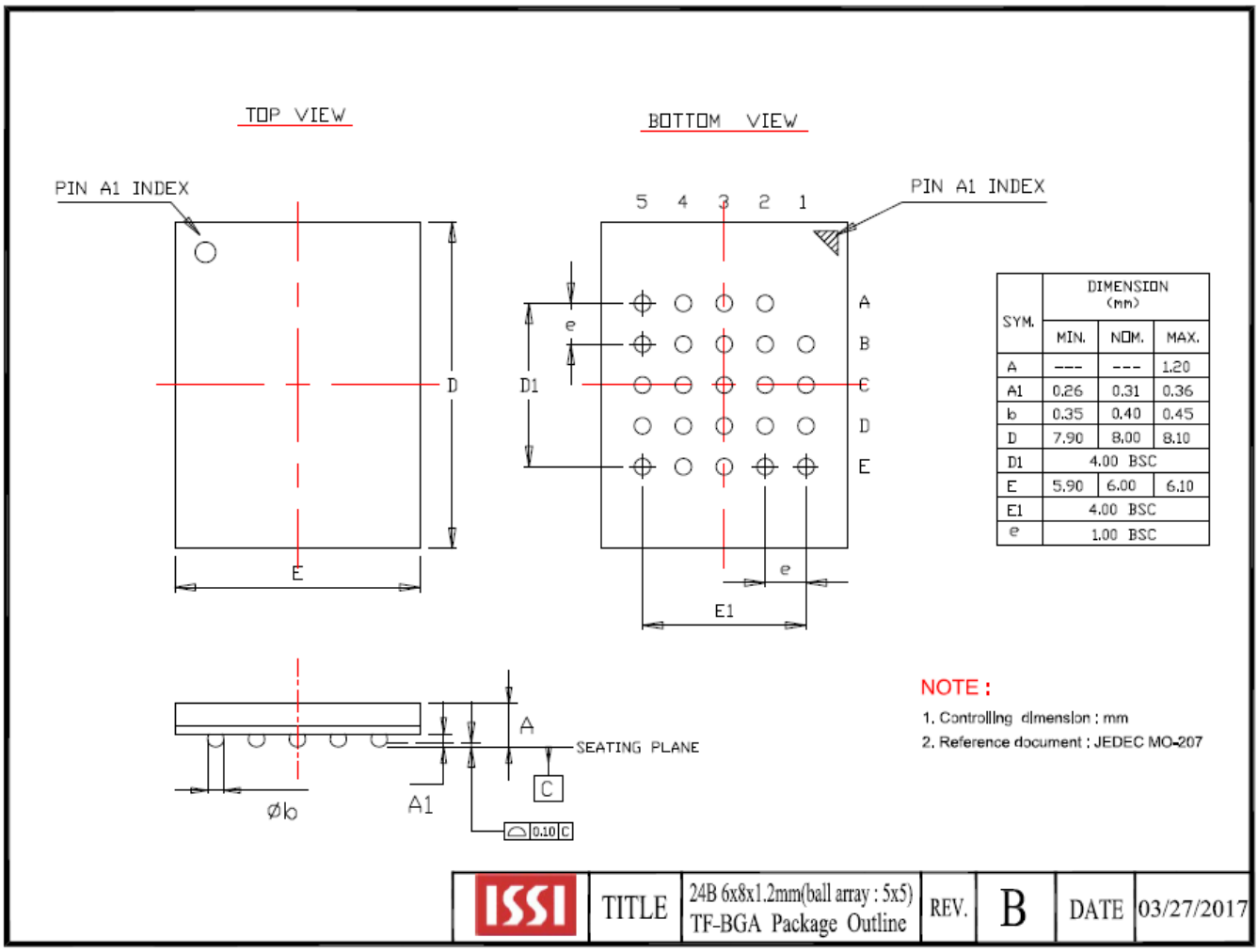
Symbol	Parameter		200MHz		166MHz		Unit
			Min.	Max.	Min.	Max.	
LC	Latency Count		7	-	6	-	clock
tRWR	Read-Write Recovery Time		35	-	36	-	ns
tCK	Clock (CLK) Period		5	-	6	-	ns
tCH	Clock High level width		0.45	-	0.45	-	tCKmin
tCL	Clock Low level width		0.45	-	0.45	-	tCKmin
tHP	Clock half period		Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid		-	12	-	12	ns
tAC	Clock transition to DQ valid	1.8V	0.9	5	1	5.5	ns
		3.0V	0.9	6.5	1	7.0	ns
tDQSCK	Clock transition to DQSM valid	1.8V	0.9	5	1	5.5	ns
		3.0V	0.9	6.5	1	7.0	ns
tCSP	CS# High Between READ/WRITE		6	-	6	-	ns
tCSS	CS# Setup to next CLK Rising Edge		3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge		2	-	2	-	ns
tSS	SDR Input Setup		0.6	-	0.9	-	ns
tSH	SDR Input Hold		0.6	-	0.9	-	ns
tDS	DDR Input Setup		0.5	-	0.6	-	ns
tDH	DDR Input Hold		0.5	-	0.6	-	ns
tDQSQ	DQSM-DQ Skew	1.8V	-	0.4	-	0.45	ns
		3.0V	-	0.4	-	0.85	
tQHS	Data Hold Skew factor	1.8V	-	0.8	-	0.90	ns
		3.0V	-	0.8	-	1.60	
tQH	DQ hold time from DQSM		tHP-tQHS	-	tHP-tQHS	-	ns
tLZ	Clock to DQ Low-Z		0	-	0	-	ns
tHZ	CS# Inactive to DQSM and DQ High-Z	1.8V	-	5	-	6	ns
		3.0V	-	6.5	-	7	
tCSM	Chip Select Maximum Low Time (~ 85°C)		-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)		-	1.0	-	1.0	us

7.6.2 WRITE Timing Parameters

Symbol	Parameter		200MHz		166MHz		Unit
			Min.	Max.	Min.	Max.	
LC	Latency Count		7	-	6	-	clock
tRWR	Read-Write Recovery Time		35	-	36	-	ns
tCK	Clock (CLK) Period		5	-	6	-	ns
tCH	Clock High level width		0.45	-	0.45	-	tCKmin
tCL	Clock Low level width		0.45	-	0.45	-	tCKmin
tHP	Clock half period		Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid		-	12	-	12	ns
tDQSCK	Clock transition to DQSM valid	1.8V	0.9	5	1	5.5	ns
		3.0V	0.9	6.5	1	7.0	ns
tCSP	CS# High Between READ/WRITE		6	-	6	-	ns
tCSS	CS# Setup to next CLK Rising Edge		3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge		2	-	2	-	ns
tSS	SDR Input Setup		0.6	-	0.9	-	ns
tSH	SDR Input Hold		0.6	-	0.9	-	ns
tDS	DDR Input Setup		0.5	-	0.6	-	ns
tDH	DDR Input Hold		0.5	-	0.6	-	ns
tDMV	Data Mask Valid (DQSM setup to end of initial latency)		0	-	0	-	ns
tCSM	Chip Select Maximum Low Time (~ 85°C)		-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)		-	1.0	-	1.0	us

8. PACKAGE TYPE INFORMATION

8.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (B)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

9. ORDERING INFORMATION – Valid Part Numbers

IS66 WVQ 16M4 F ALL - 200 B L I

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE Type (1)
B = 24-ball TFBGA 6x8mm 5x5 ball array
W = KGD (Call Factory)

Frequency
200 = 200MHz
166 = 166MHz

VDD
ALL = 1.8V
BLL = 3.0V

Die Revision
F = die rev F

Density/Org.
16M4 = 16Mbx4=64Mb

PSRAM Product Type.
WVQ = QuadRAM

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
66 = PSRAM
67 = PSRAM for Automotive

Industrial Temperature Range (-40°C to +85°C)

Config.	Voltage	Max. Frequency (MHz)	Order Part Number(1)	Package
16Mbx4	1.8V	200	IS66WVQ16M4FALL-200BLI	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS66WVQ16M4FALL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	200	IS66WVQ16M4FBLL-200BLI	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS66WVQ16M4FBLL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array

Automotive A2 Temperature Range (-40°C to +105°C)

Config.	Voltage	Max. Frequency (MHz)	Order Part Number(1)	Package
16Mbx4	1.8V	200	IS67WVQ16M4FALL-200BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS67WVQ16M4FALL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	200	IS67WVQ16M4FBLL-200BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS67WVQ16M4FBLL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array