

512Mb SPI OctalRAM (x16)

Advanced Information

Overview

The IS66/67WVX32M16EALL/BLL are integrated memory device containing 512Mb Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 32M words by 16 bits.

The device supports Octal Peripheral Interface (Address, Command through 8 pins, and Data through 16 pins), Very Low Signal Count (20 signal pins; SCLK, CS#, DQSM[1:0], SIO[7:0] and SIO[15:8]), Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Key Features

- **Industry Standard Serial Interface**
 - Octal Peripheral Interface (OPI) Protocol
 - Low Signal Counts: 20 Signal pins (CS#, SCLK, DQSM[1:0], SIO[15:0])
- **Supply Voltage**
 - VCC = 1.7V ~1.95V (ALL), 2.7V~3.6V (BLL)
- **DDR Operation**
 - Two bytes transfer per clock (x8)
 - Two words transfer per clock (x16)
- **Performance**
 - Up to 200MHz (800MB/s – x16, 400MB/s – x8)
- **Organization**
 - Mode register configurable **x8 (default)/x16**
- **Features**
 - Data strobe for high speed Read Operation.
 - Data Mask during Write Operation
 - Configurable Latency for Read/Write Operation)
 - Supports Variable Latency mode and Fixed Latency mode
 - Configurable Drive Strength
 - Supports Wrapped Burst and Hybrid Burst
 - Continuous Burst (Linear Burst) Commands
 - No limitation in Row Boundary Crossing
- **Wrap & Hybrid Burst length**
 - 16/32/64/2K Bytes length in x8 mode
 - 16/32/64/1K Words length in x16 mode
- **Hardware Features**
 - SCLK Input: Clock input
 - SIO[7:0]: Command/Address/Data bus
 - SIO[15:8] : Data bus
 - DQSM[1:0]:
 - Output during read data transactions as Read Data Strobe
 - Input during write data transactions as Write Data Mask
 - RESET#: Hardware Reset pin
- **Low Power Features**
 - Partial Array Self Refresh (PASR)
 - Supports Deep Power Down mode
 - Ultra Low Power Hybrid Sleep mode with data retained.
- **Temperature Grades**
 - Industrial: -40°C to +85°C
 - Auto (A1) Grade: -40°C to +85°C
 - Auto (A2) Grade: -40°C to +105°C
- **Industry Standard PACKAGE**
 - A = 49-ball TFBGA 8x8mm 7x7 Array
 - B = 24-ball TFBGA 6x8mm 5x6 Array
 - KGD (Call Factory)
 - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

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1. General Description

The IS66/67WVX32M16EALL/BLL are integrated memory device containing 512Mb Pseudo Static Random Access Memory using a self-refresh DRAM array can be organized as 32M words by 16 bits [after mode register setting](#) (Default organization is 64M words by 8 bits after power up).

The device supports Octal Peripheral Interface (Address, Command through 8 pins, and data through 16 pins) , Very Low Signal Count (20 signal pins; SCLK, CS#, DQSM[1:0], SIO[7:0] and SIO[15:8]), Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Due to DTR operation, minimum data size is double byte (32-bit) based instead of byte (16-bit) base.

Performance Summary

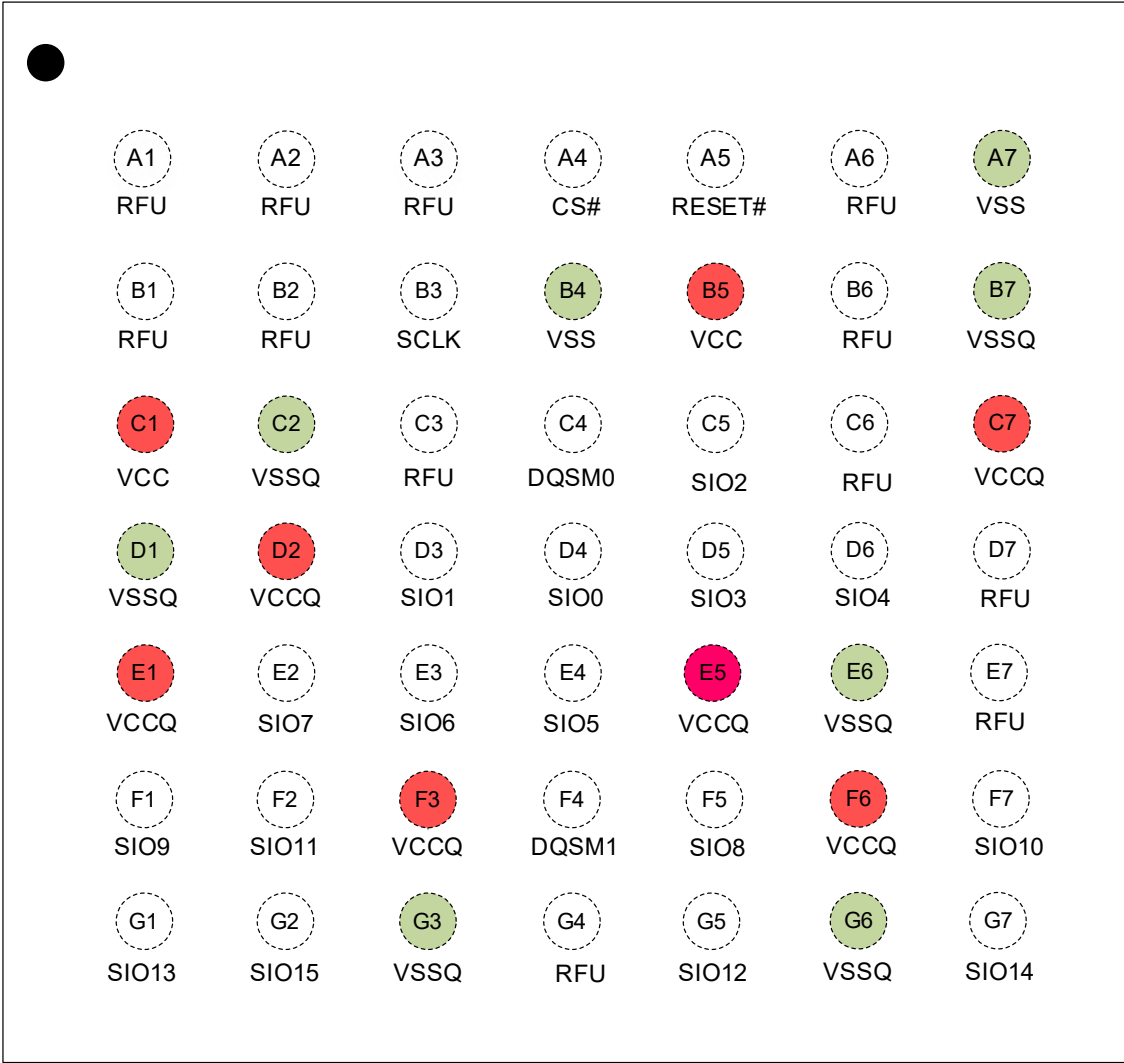
Read / Write Operation	
Maximum Clock Rate	200MHz

Maximum Current Consumption	
VCC Active Read Current	35 mA
VCC Active Write Current	35 mA
Standby (Full Array, 105°C)	1800 uA
Half Sleep (Full Array, 105°C)	1000 uA
Deep Power Down (105°C)	80 uA

2. PIN CONFIGURATION

49-ball TFBGA (8mm x 8mm, 7x7 ball array, Package Code: A)

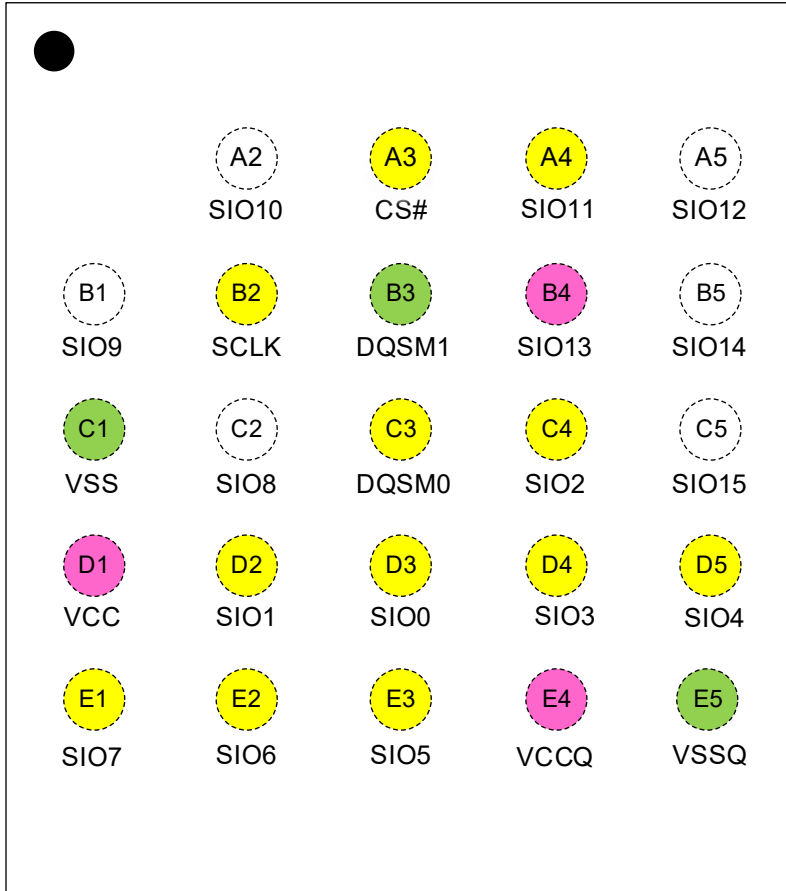
Top View, Balls Facing Down



 VCC, VCCQ
  VSS, VSSQ

24-ball TFBGA (6mm x 8mm, 5x5 ball array, Code: B)

Top View, Balls Facing Down



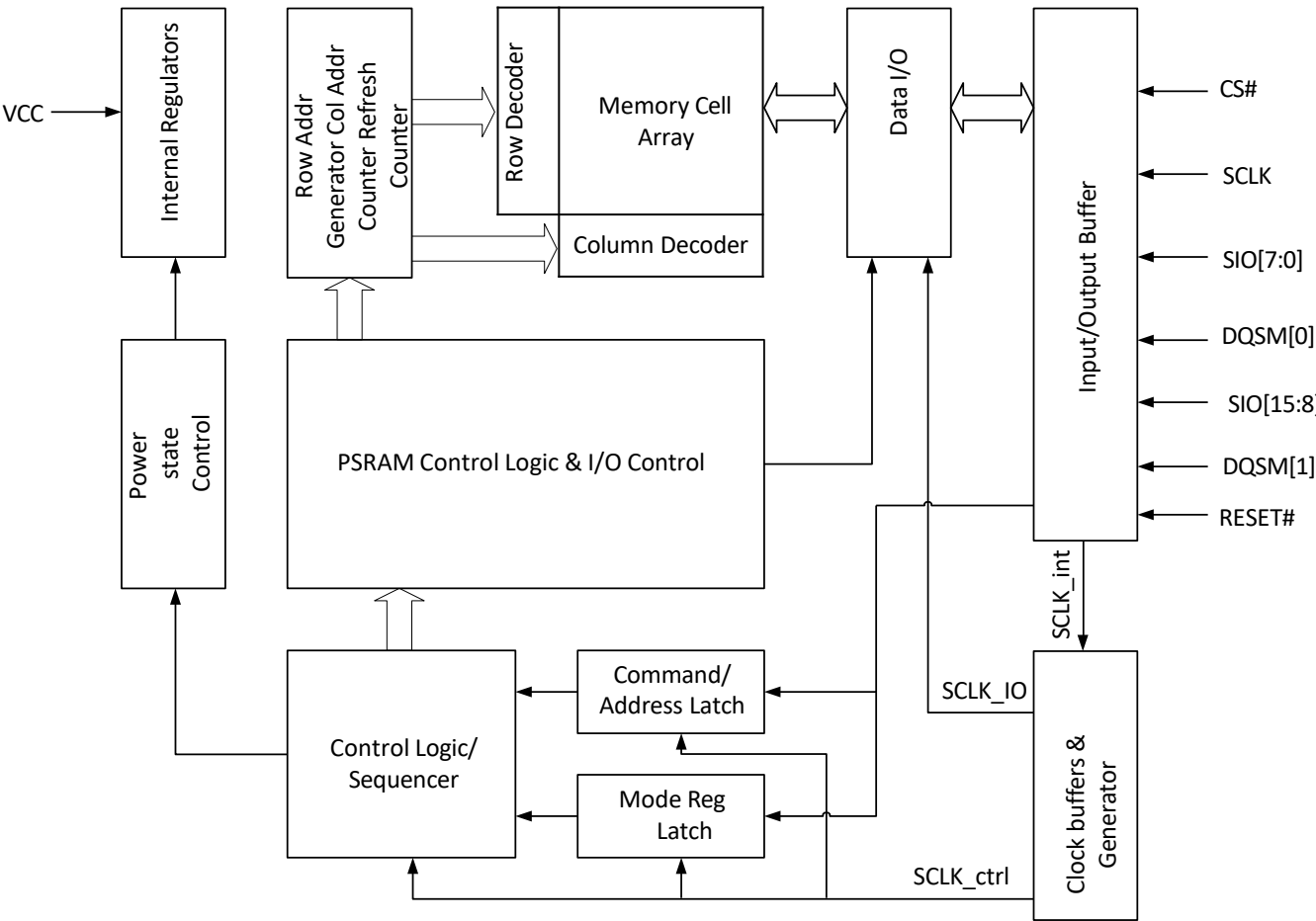
3. Signal Descriptions

All signals for the device are listed below in Table 3.1.

Table 3.1. Signal Descriptions

Symbol	Type	Description
VCC	Power Supply	Power Supply
VCCQ	Power Supply	IO Power Supply, Available for 49 BGA only.
VSS	Power Supply	Ground
VSSQ	Power Supply	IO Ground, Available for 49 BGA only.
SIO[15:0]	IO	Serial Data Input & Output pins.
DQSM[1:0]	IO	Data Strobe Signal in Read operation, and Write Data Mask in Write operation: DQSM[0] for SIO[7:0] , and DQSM[1] for SIO[15:8].
CS#	Input	Chip select, active low. When CS#=1, chip is in standby state.
RESET#	Input	The RESET# pin is a hardware RESET signal. When RESET# is driven High, the memory is in the normal operating mode. When RESET# is driven Low, the memory enters reset mode and output is High-Z. It has an internal pull-up register and may be left floating if not used. Available for 49 BGA only.
SCLK	Input	Serial Data Clock: Synchronized Clock for input and output timing operations.
RFU	Unused	Reserved for Future Use.

4. Functional Diagram



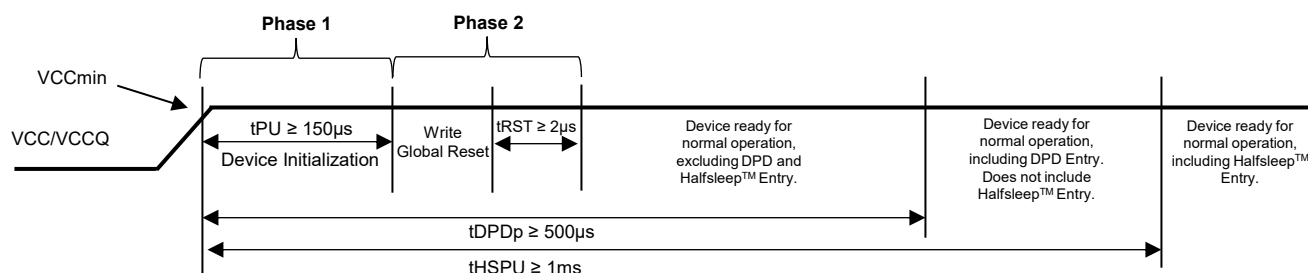
5. Power-Up Initialization

The device includes an on-chip voltage sensor used to start the self-initialization process. When the device reaches a stable level at or above minimum VCC, the device is in Phase 1 and it requires 150us to complete its self-initialization process. The host can proceed to [optional](#) Phase 2 of the initialization.

During Phase1, CS# should remain HIGH (track VCC within 200mV); SCLK should remain LOW.

After Phase1 or optional Phase 2 is complete, the device is ready for operation, however Hybrid Sleep entry and Deep Power Down (DPD) entry are not available until Hybrid Sleep Power Up (tHSPU) or DPD Power Up (tDPDp) durations are observed.

Figure 5.1: Power-Up & Device Initialization Timing with Global Reset

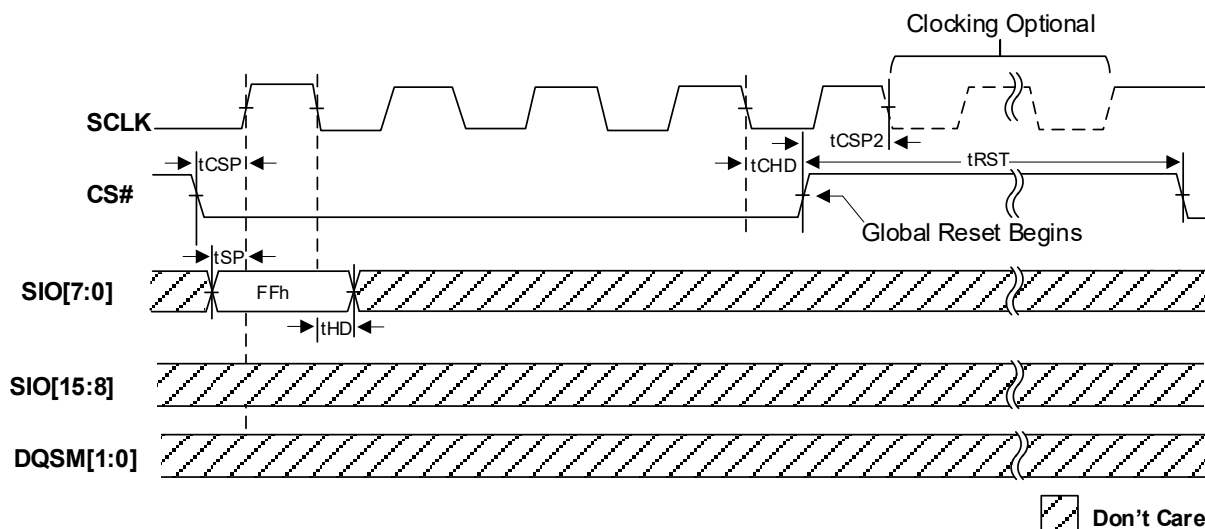


5.1 Power-Up Initialization Method via. Global Reset

Global Reset command is a power-up initialization method. After the Phase 1 of 150 us period, the host can issue Global Reset command to reset the device.

Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CS# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below. **Global Reset operation is an optional operation for unstable VCC ramp up environment, and it can be skipped if VCC ramp up is stable. The device can be used after POWER ON Device Initialization (after phase 1).**

Figure 5.2: Global Reset command sequence



6. Interface Description

6.1 Address Space

The device is **byte-addressable (x8, default)/word-addressable (x16)**. Memory accesses must start on even address (A[0]=0). Mode Register accesses can start on even or odd address.

6.2 Burst Type & Length

Read and write operations are default Hybrid Wrap 32 mode. Burst lengths of 16, 32, 64, 128 and 1K words in standard or Hybrid wrap modes are register configurable (16, 32, 64, 128 and 2K bytes configurable in x8 mode). The device also includes command burst options for Linear Bursting. Bursts can start on any even address. Write burst length requires a minimum of 2 words (x16)/2 bytes (x8).

Read has no minimum length.

Both write and read have no restriction on maximum burst length as long as tCEM is met.

6.3 Command/ Address Latching

After CS# goes LOW, the command is latched on the 1st SCLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th SCLK edges. (2nd SCLK rising edge, 2nd SCLK falling edge, 3rd SCLK rising edge, 3rd SCLK falling edge).

6.4 Command Truth Table

The device recognizes command listed in the following table. Command and address are input through SIO[7:0] pins. Host must send correct command and address format according to the following table.

Command	1st SCLK		2nd SCLK		3rd SCLK	
Read	00h		A3	A2	A1	A0
Write	80h		A3	A2	A1	A0
Linear Burst Read	20h		A3	A2	A1	A0
Linear Burst Write	A0h		A3	A2	A1	A0
Mode Register Read	40h		X			MA
Mode Register Write	C0h		X			MA
Global Reset	FFh		X			

	Standard		Gapless Address		Remark
	X8	X16	X8	X16	
A3	RA[14:13]		RA[14:13]	RA[14]	Unused address bits are reserved
A2	RA[12:5]		RA[12:5]	RA[13:6]	
A1	RA[4:0], CA[10:8]	RA[4:0] , CA[9:8]	RA[4:0], CA[10:8]	RA[5:0], CA[9:8]	7 address bits for x16 Standard
A0	CA[7:0]				
MA = Mode Register Address, X= don't care (V _{IH} /V _{IL})					

Notes:

- CA10 is only used in x8 mode.
- Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0].
- Both Linear Burst Read command and Linear Burst Write command are capable of performing row boundary crossing function.
- Contact ISSI Marketing for x16 Gapless Address.

6.5 Read Operation

Output data is available after predefined latency cycles. LC is latency count code defined in Table 6.3 and Table 6.4. When data is valid, SIO and DQSM follow the timing specified in Figure 6.2. Synchronous timing parameters are shown in Table 8.1.

In case of internal refresh collision, variable latency output data may be delayed to 2LC latency cycles as shown in Figure 6.2. The 1st DQSM rising edge after read pre-amble indicates the beginning of valid data.

In x16 mode, SIO[15:8] will be don't care during Command/Address cycles, and will start driving output data after latency cycles, similar to SIO[7:0] .

Figure 6.1: Read Operation Timing (Variable Latency, No Refresh Collision)

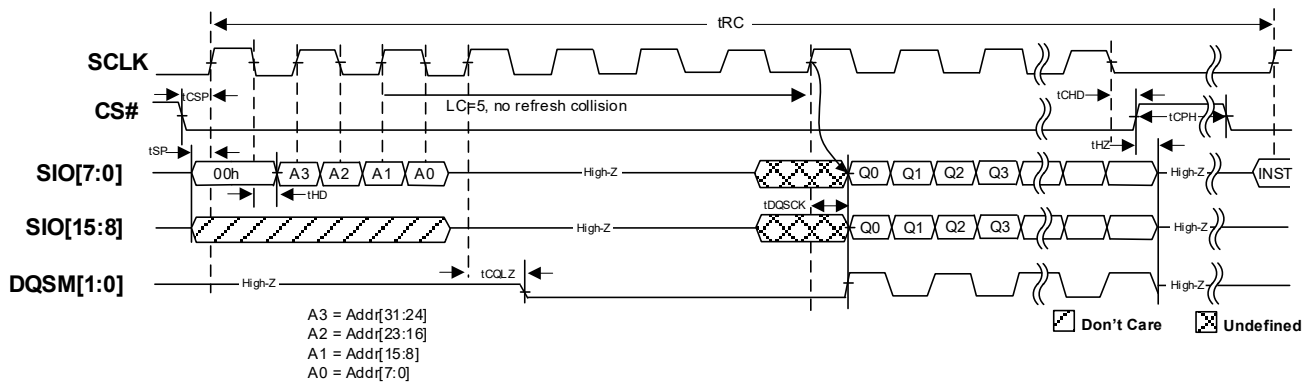


Figure 6.2: Read Operation Timing (Variable Latency, Refresh Collision)

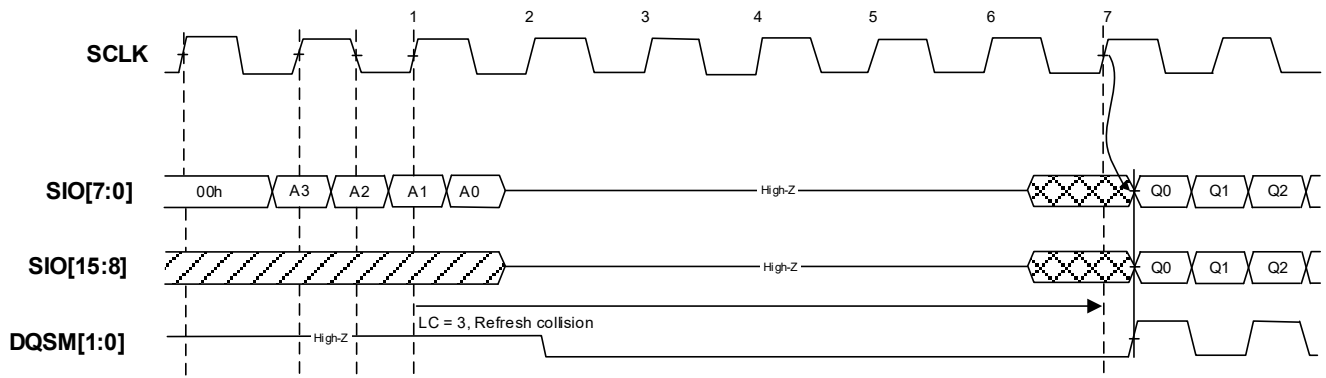
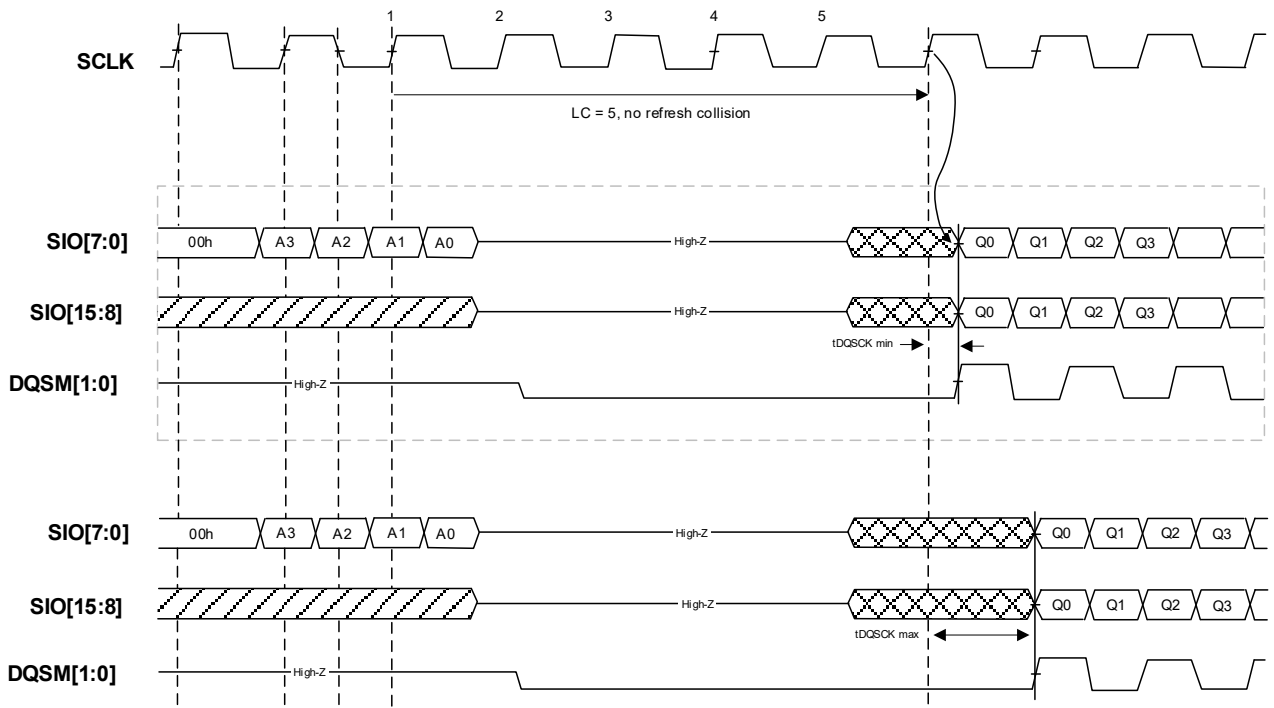
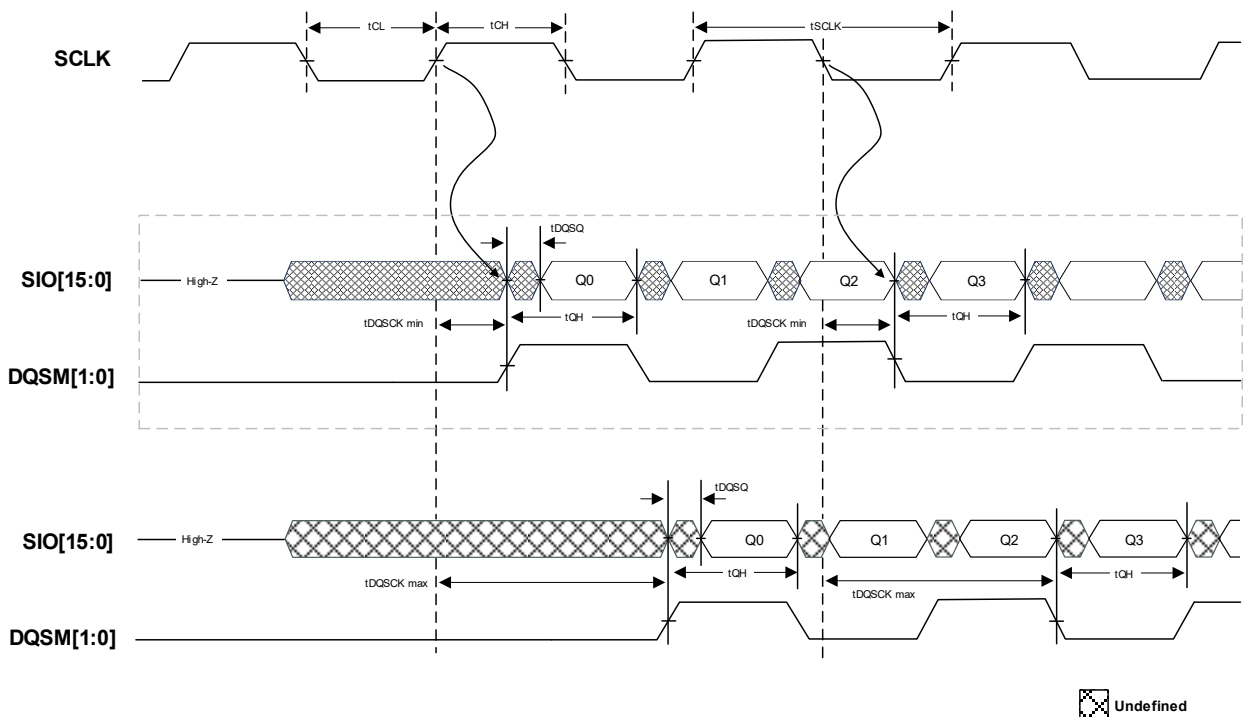


Figure 6.3: SCLK & DQSM Timing in Read Operation

Figure 6.4: Output Data & DQSM Timing in Read Operation

Notes :

1. All Output Data (Qn) are valid t_{DQSQ} after the DQSM edge, regardless of t_{DQSK} .
2. DQSM[0] is for SIO[7:0], DQSM[1] is for SIO[15:8]

6.6 Write Operation

A minimum of 2 bytes (in x8 mode) / 2 words (in x16 mode) of data must be input in a write operation. In the case of consecutive short burst writes, t_{RC} must be met by issuing additional CS# high time between operations. Single byte write operations can be done by masking through DQSM pin.

In x16 mode, SIO[15:8] are ignored during Command/Address cycles. Instead, SIO[15:8] are only used after write latency to receive the data, similar to SIO[7:0]. During write data cycles, the SIO[15:8] and SIO[7:0] can be independently masked via DM[1] and DM[0].

Figure 6.5: Write Operation Timing

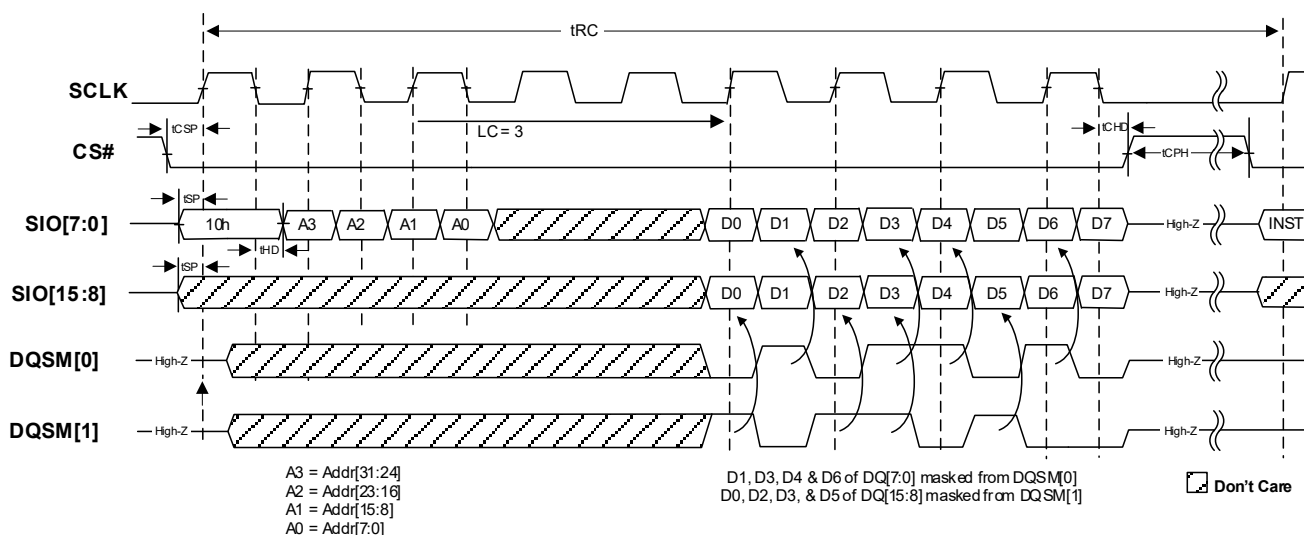
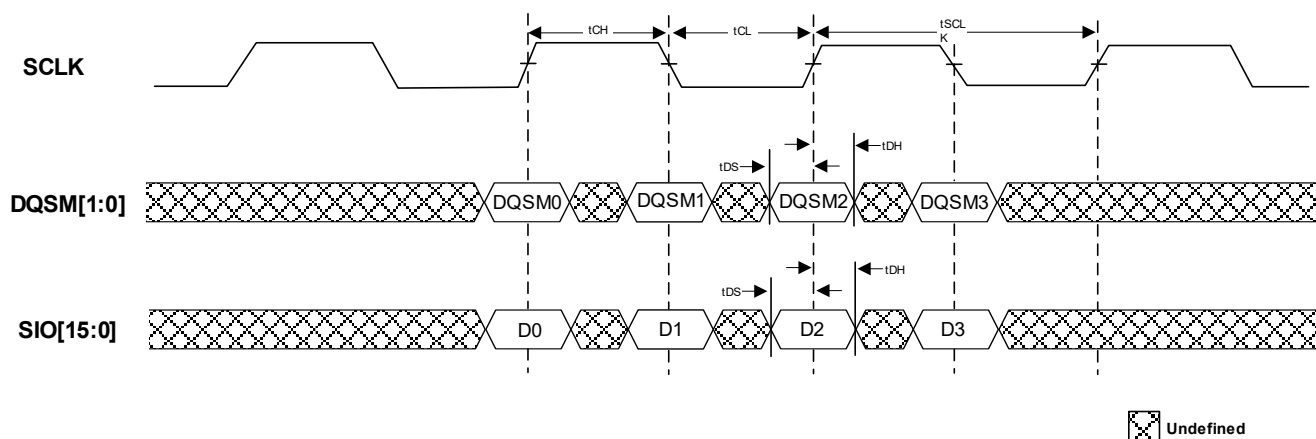


Figure 6.6: Input Data & DQSM Timing in Write Operation



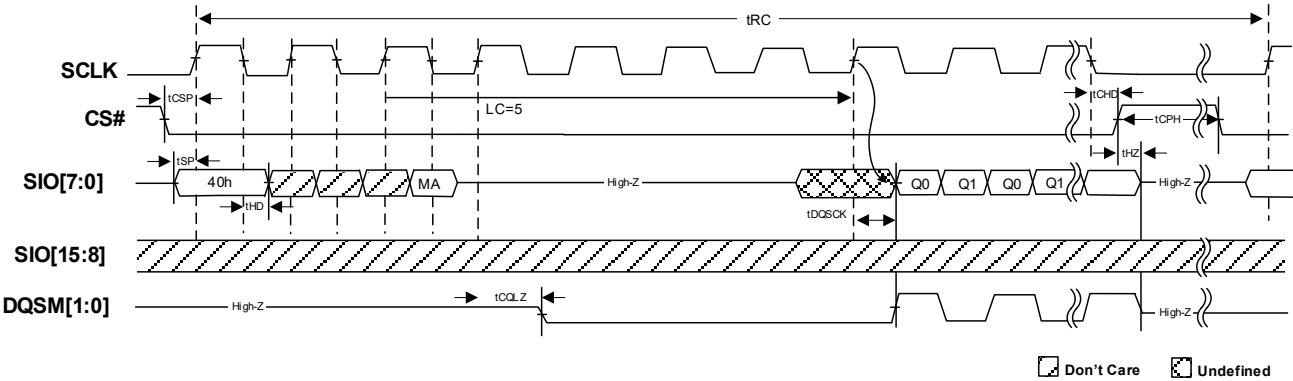
Notes :

1. DQSM[1] is DQSM for SIO[15:8]
2. DQSM[0] is DQSM for SIO[7:0]

6.7 Mode Registers Read & Write

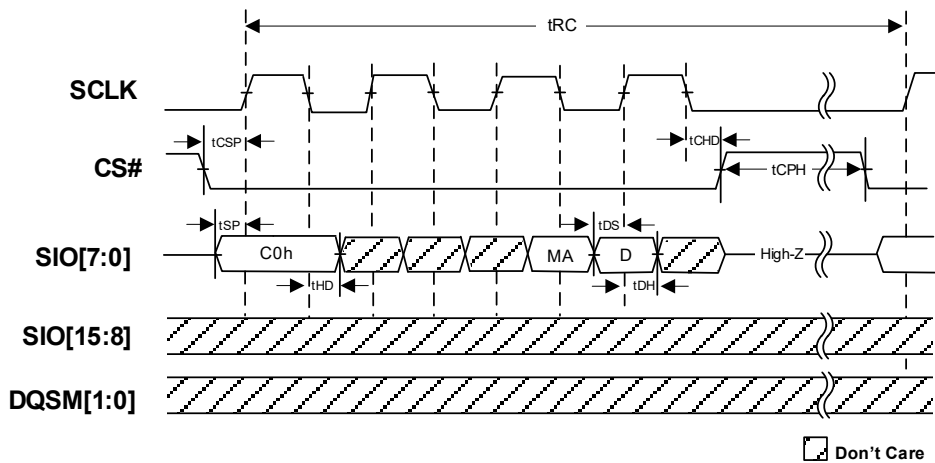
MA (Mode Register Address) in command determines which Mode Register to be selected. All Mode Registers (MR0~MR8) are 8-bit wide, Mode Register write and read uses only SIO[7:0], and unused SIO[15:8] are don't care. Mode Register read is shown below in Figure 6.7. The latency count for Mode Register read operation is always LC, defined in MR0[4:2], regardless of MR0[5] setting. When MA is 00h, MR0 data is available after LC cycles, at the rising edge of SCLK, followed by MR1 data at the falling edge of SCLK, and both data are repeated until CS# goes to HIGH. Mode registers 0, 4 & 8 are read and writable. Registers 1, 2 and 3 are read only. MA and corresponding mode register data pair is described as below Table 6.1.

Figure 6.7: Mode Register Read



MA	00h	01h	02h	03h	04h	08h
First Data (Q0)	MR0	MR1	MR2	MR3	MR4	MR8
Second Data (Q1)	MR1	MR2	MR3	MR4	MR8	MR0

Figure 6.8: Mode Register Write



Latency count for Mode Register write operation is always 0. When MA is 00h, MR0 data will be written at the rising edge of next SCLK.
 Registers 0, 4 & 8 are read and writable. Register 6 is write only.
 MR0[7:6], MR6[3:0], and MR8[7] must be written to '0's).

Table 6.1: Mode Register Table

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	R/W	00		LT	Read Latency Count			Drive Strength	
1	01h	R	ULP	Rsvd		Vendor ID				
2	02h	R	KGD			Device ID		Density		
3	03h	R	Rsvd	0	SRF		Rsvd			
4	04h	R/W	Write Latency Count			RF Rate		PASR		
6	06h	W	Ultra Low Power Mode				0000			
8	08h	R/W	0	X8/x16	Rsvd			BT	BL	

Table 6.2: Read Latency Type MR0[5]

Latency Type	
MR0[5]	Latency Type
0	Variable (default)
1	Fixed

Table 6.3: Read Latency Count MR0[5:2]

MR0[4:2]	Variable Latency (MR0[5]=0)		Fixed Latency (MR0[5]=1)	Max Freq (MHz)
	No refresh Collision (LC)	Refresh Collision (2xLC)	Latency (2xLC)	
000	3	6	6	66
001	4	8	8	109
010	5 (default)	10	10	133
011	6	12	12	166
100	7	14	14	200
101	8	16	16	200
others	reserved			-

Table 6.4: Operation Latency Count

Type	Operation	Variable Latency (default)		Fixed Latency
		No Refresh Collision	Refresh Collision	
Memory	Read	LC	2xLC	2xLC
	Write	WLC		WLC
Register	Read	LC		LC
	Write	0		0

Note:

- See table 6.13 for WLC settings.

Table 6.5: Drive Strength Code MR0 OP[1:0]

MR4 OP[1:0]	Drive Strength
00	Full (25 ohm, default)
01	Half (50 ohm)
10	¼ (100 ohm)
11	Reserved

Table 6.6: Ultra Low Power Device mapping MR1 OP[7]

MR1 OP[7]	ULP
0	reserved
1	ULP (Hybrid Sleep supported)

Table 6.8: Vendor ID mapping MR1 OP[4:0]

MR1 OP[4:0]	Vendor
00011	ISSI

Table 6.9: Good-Die Bit MR2 OP[7:5]

MR2 OP[7:5]	Good Die ID
110	Pass
others	Fail

Table 6.10: Device ID MR2 OP[4:3]

MR2 OP[4:3]	Device ID
00	Generation 1 (default)
others	reserved

Table 6.11: Device Density mapping MR2 OP[2:0]

MR2 OP[2:0]	Density
111	256Mb
110	512Mb
010	1Gb
others	reserved

Table 6.12: Self Refresh Flag MR3 OP[5:4]

MR3 OP[5:4] (read only)	Self refresh Flag
01	0.5x refresh
00	1.0x refresh
10	4.0x refresh
11	reserved

MR3 OP[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration, set my MR4 [4:3].

Table 6.13 : Write Latency Count MR4 OP[7:5]

MR4 OP[7:5]	Write Latency Count (WLC)	Max. Frequency (MHz)
000	3	66
100	4	109
010	5 (default)	133
110	6	166
001	7	200
101	8	200
All others	Reserved	-

Write latency, WLC, is default to 5 after power up. Use MR write to set write latencies according to write latency table. When operating frequency exceeding Max. frequency listed in the table will result in write data corruption.

Table 6.14 : Refresh Frequency setting MR4 OP[4:3]

MR4 OP[4:3]	Refresh Frequency
x0	Always 4x Refresh (default)
01	Enables 1.0x refresh when temperature allows
11	Enables 0.5x refresh when temperature allows

Note:

1. X = don't care

Table 6.15: PASR MR4 [2:0]

512Mb		
Codes	Refresh Coverage	Density
000	Full array (default)	512Mb
001	Bottom 1/2 array	256Mb
010	Bottom 1/4 array	128Mb
011	Bottom 1/8 array	64Mb
100	None	0Mb
101	Top 1/2 array	256Mb
110	Top 1/4 array	128Mb
111	Top 1/8 array	64Mb

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array.

Table 6.16 : Ultra Low Power Mode MR6 OP[7:0]

MR6 OP[7:0]	Ultre Low Power Mode
F0h	Hybrid Sleep
C0h	Deep Power Down
others	Reserved

Table 6.17 : IO x8/x16 Mode MR8 OP[6]

MR6 OP[7]	X8/x16 Mode
0	X8 (default) ⁽¹⁾
1	X16

Device powers up in x8 mode, MR8 OP[6] = 0. After power up device can be configured to x16 mode by setting MR8 OP[6]=1 via mode register write command. Host can switch in and out of x8 mode any time after power up.

Note:

- 1. Contact ISSI MKT for x16 default after power up.

Table 6.18 : Burst Type MR8 OP[2], Burst Length MR8 OP[1:0] in x8 Mode

MR8 OP[2]	MR8 OP[1:0]	Burst Length	Example of Sequence of Bytes During Wrap	
			Starting	Burst Address Sequence in x8 Mode
0	00	16 Byte	4	[4, 5, 6,...15, 0, 1, 2,...]
0	01	32 Byte	4	[4, 5, 6,...31, 0, 1, 2,...]
0	10	64 Byte	4	[4, 5, 6,...63, 0, 1, 2,...]
0	11	2K Byte	4	[4, 5, 6,...2047, 0, 1, 2,...]
1	00	16 Byte	2	[2, 3, 4,...15, 0, 1], 16, 17, ...2047, 2048,...
1	01	32 Byte	2	[2, 3, 4,...31, 0, 1], 32, 33, ...2047, 2048,...
1	10	64 Byte	2	[2, 3, 4,...63, 0, 1], 64, 65, ...2047, 2048,...
1	11	2K Byte	2	[2, 3, 4,...2047, 0, 1], 2048, 2049, 2050,...

Table 6.19 : Burst Type MR8 OP[2], Burst Length MR8 OP[1:0] in x16 Mode

MR8 OP[2]	MR8 OP[1:0]	Burst Length	Example of Sequence of Words During Wrap	
			Starting	Burst Address Sequence in x16 Mode
0	00	16 Word	4	[4, 5, 6,...15, 0, 1, 2,...]
0	01	32 Word	4	[4, 5, 6,...31, 0, 1, 2,...]
0	10	64 Word	4	[4, 5, 6,...63, 0, 1, 2,...]
0	11	1K Word	4	[4, 5, 6,...1023, 0, 1, 2,...]
1	00	16 Word	2	[2, 3, 4,...15, 0, 1], 16, 17, ...1023, 1024,...
1	01	32 Word	2	[2, 3, 4,...31, 0, 1], 32, 33, ...1023, 1024,...
1	10	64 Word	2	[2, 3, 4,...63, 0, 1], 64, 65, ...1023, 1024,...
1	11	1K Word	2	[2, 3, 4,...1023, 0, 1], 1024, 1025, 1026,...

By default the device powers up in 32 Byte Hybrid Wrap in x8 mode/ 32 Word Hybrid Wrap in x16 mode). In non-Hybrid burst (MR8 OP[2]=0), MR8 OP[1:0] sets the burst address space in which device will continually wrap within. If Hybrid burst wrap is selected (MR8 OP[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally to the last array address to the first address.

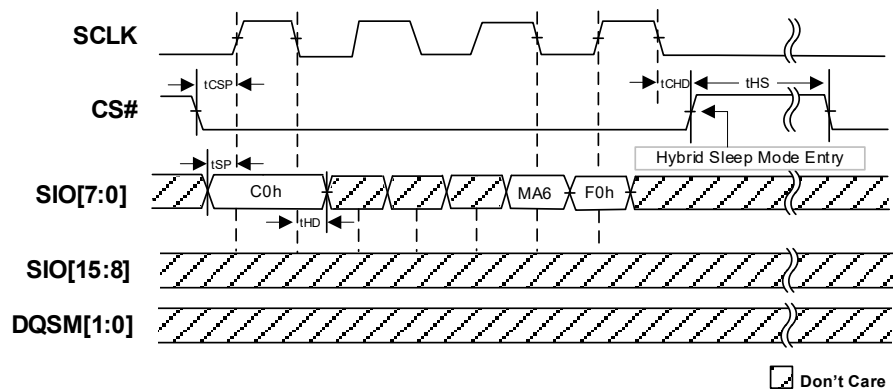
Burst length (MR8 OP[1:0] can be set to 16, 32, 64 & 2K in x8 mode (16, 32, 64 & 1K in x16 mode) lengths.

The Linear Burst commands (20h for read, A0h for write) force the current array read or write to continue even after the last array address to the first address.

6.8 Hybrid Sleep Mode

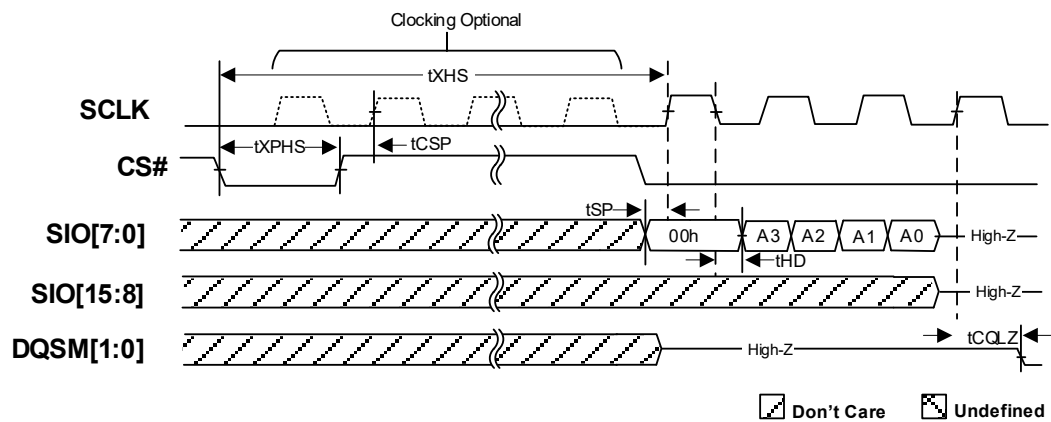
Hybrid Sleep mode puts the device in an ultra-low power state, while the stored data is retained. Hybrid Sleep mode Entry is entered by writing F0h into MR6. CS# going high initiates the Hybrid Sleep mode and must be maintained for the minimum duration of Hybrid Sleep time, tHS.

Figure 6.9: Hybrid Sleep Entry Write (latency same as Register Write)



Hybrid Sleep Exit is initiated by a low pulsed CS#. Afterwards, CS# can be held high with or without clock toggling until the first operation begins (observing minimum Hybrid Sleep Exit time, tXHS).

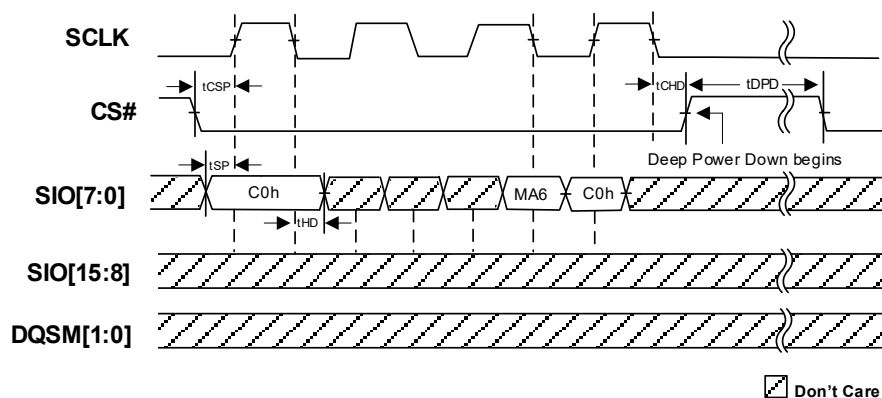
Figure 6.10: Hybrid Sleep Exit followed by read operation.



6.9 Deep Power Down Mode

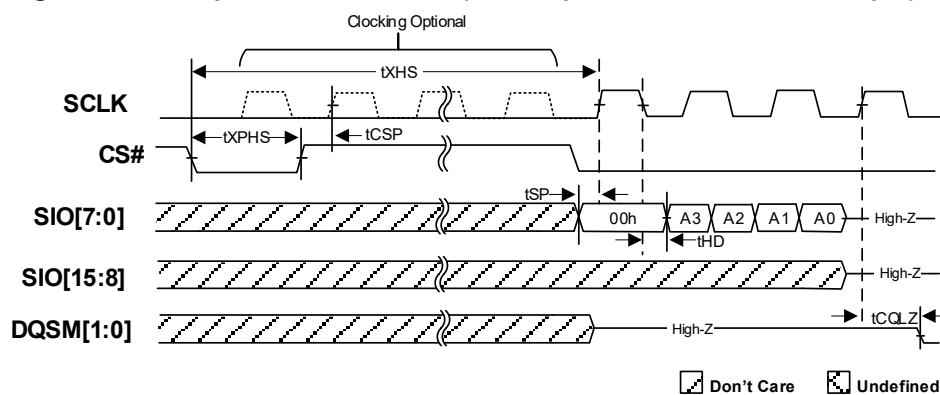
Deep Power Down (DPD) mode puts the device into power down state. DPD Entry is entered by writing C0h into MR6. CS# going high initiates the Hybrid Sleep mode and must be maintained for the minimum duration of Deep Power Down time, tDPD.

Figure 6.11: Deep Power Down Entry Write (latency same as Register Write)



Deep Power Down Exit is initiated by a low pulsed CS#. After DPD exit, CS# must be held high with or without clock toggling until the first operation begins (observing minimum Deep Power Down Exit time, tXDPD).

Figure 6.12: Deep Power Down Exit (Read Operation shown as example)



Register values and memory content are not retained in DPD mode. After DPD mode, register values will reset to defaults. tDPD is minimum period between two DPD modes (measured from DPD exit to the next DPD entry) as well as from the initial power up to the first DPD entry.

6.10 Partial-array self refresh

Partial-array self refresh (PASR) mode is a feature which puts the device into a power-saving state while keeping the memory array restricts refresh operation to a portion of the total memory array.

Partial-array self refresh (PASR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array that is absolutely necessary. The refresh options are full array, 1/2 array, 1/4 array, and selected by MR7 OP[3:2].

Data stored in addresses not receiving refresh will become corrupted.

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7.1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on any ball relative to VSS, except VCC, VCCQ	VT	-0.5 to +VCC/VCCQ+0.5	V	
Power supply VCC relative to VSS	VCC	-0.5 to +VCC+0.5	V	
Power supply VCCQ relative to VSSQ	VCCQ	-0.5 to +VCCQ+0.5	V	
Storage temperature	T _{STG}	-55 to +125	°C	1
Power Dissipation	PD	1.0	W	

Note:

1) Storage temperatures refers to the case surface temperature on the center/top side of the device.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in operational section of the specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

7.2 Pin Capacitance

Table 7.2: Package Pin Capacitance

Parameter	Symbol	Min.	Max.	Unit	Notes
Input Pin Capacitance	CIN	-	5	pF	VIN = 0V
Output Pin Capacitance	COUT	-	6	pF	VOUT = 0V

Table 7.3: Load Capacitance

Parameter	Symbol	Min.	Max.	Unit	Notes
Load Capacitance	CL	-	15	pF	

7.3 Operating Temperature

Table 7.4: Operating Temperature

Grade	Min.	Max.	Unit	Notes
Industrial	-40	85	°C	
Automotive A1	-40	85	°C	
Automotive A2	-40	105	°C	

7.5 DC Characteristics

Table 7.5: Operating Temperature

Symbol	Parameter		Min.	Max.	Unit	Note
VCC	Supply Voltage	ALL	1.7	1.95	V	
		BLL	2.7	3.60		
VCCQ	I/O Supply Voltage	ALL	1.7	1.95	V	
		BLL	2.7	3.60		
VIH	Input HIGH voltage		VCCQ - 0.4	VCCQ + 0.4	V	
VIL	Input LOW voltage		-0.3	0.4	V	
VIH	Output HIGH voltage		0.8 x VCCQ	-	V	
VIL	Output LOW voltage		-	0.2 x VCCQ	V	
ILI	Input Pin leakage current		-	1	uA	
ILO	Output Pin leakage current		-	1	uA	
ICC	Read/Write @133MHz		-	TBD	mA	1
	Read/Write @166MHz		-	TBD	mA	1
	Read/Write @200MHz		-	35	mA	1
ISB	Standby current (Full Array)	85°C	-	1500	uA	2
		105°C	-	1800	uA	2
IDPD	Deep Powr Down current (Full Array)	85°C	-	50	uA	3
		105°C	-	80	uA	3
IHS	Hybrid Sleep current (Full Array)	85°C	-	800	uA	
		105°C	-	1000	uA	

Notes:

- 1) Current is only characterized.
- 2) Without SCLK toggling. ISB will be increased if SCLK is toggling.
- 3) Typical IDPD is 30 mA at 25°C.

7.6 ISB /IHS Partial Array Current

Table 7.6: Typical PASR Current at 25°C

PASR	ISB-typical	IHS-typical ⁽³⁾	Units	Notes
Full Array	TBD	TBD	uA	1, 2
1 / 2 Array	TBD	TBD	uA	1, 2
1 / 4 Array	TBD	TBD	uA	1, 2
1 / 8 Array	TBD	TBD	uA	1, 2

Table 7.7: Maximum PASR Current at 85°C

PASR	ISB-maximum	HIS-maximum ⁽³⁾	Units	Notes
Full Array	1500	800	uA	1, 2
1 / 2 Array	1200	600	uA	1, 2
1 / 4 Array	1000	500	uA	1, 2
1 / 8 Array	800	400	uA	1, 2

Table 7.8: Maximum PASR Current at 105°C

PASR	ISB-maximum	HIS-maximum ⁽³⁾	Units	Notes
Full Array	1800	1000	uA	1, 2
1 / 2 Array	1600	800	uA	1, 2
1 / 4 Array	1400	600	uA	1, 2
1 / 8 Array	1200	500	uA	1, 2

Notes:

- 1) Current at 25°C is only attainable by enabling 0.5 x Refresh Frequency
- 2) PASR current is only characterized without SCLK toggling.
- 3) IHS is only guaranteed after 150ms into Hybrid Sleep mode.

8. AC Characteristics

Table 8.1: READ/WRITE Timing Parameters

Symbol	Parameter		133MHz		166MHz		200MHz		Unit	Notes
			Min	Max	Min	Max	Min	Max		
tCLK	CLK Period		7.5		6		5		ns	
tCH/tCL	CLK high/low width		0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHKL	CLK rise or fall time		-	1.2	-	1.0	-	0.8	ns	
tCPH	CS# high between subsequent burst operations		15	-	18	-	24	-	ns	
tCEM	CS# low pulse width	85°C	-	4	-	4	-	4	us	2
		105°C	-	1	-	1	-	1	us	2
tCPL	CS# low pulse width		3	-	3	-	3	-	tCLK	
tCSP	CS# setup time to SCLK rising edge		2.5	-	2.5	-	2.5	-	ns	
tCSP2	CS# rising edge to next SCLK falling edge		1.5	-	1.5	-	1.5	-	ns	
tCHD	CS# hold time from SCLK falling edge		2	-	2	-	2	-	ns	
tSP	Setup time to active SCLK edge		0.8	-	0.6	-	0.5	-	ns	
tHD	Hold time from active SCLK edge		0.8	-	0.6	-	0.5	-	ns	1
tHZ	Chip disable to DQ/DQS output		-	6	-	6	-	6	ns	
tRC	Read/Write Cycle		60	-	60	-	60	-	ns	
tHS	Min. Hybrid Sleep duration		150	-	150	-	150	-	us	
tXHS	Hybrid Sleep Exit CS# low to SCLK setup time		150	-	150	-	150	-	us	
tXPHS	Hybrid Sleep Exit CS# low pulse width		60	-	60	-	60	-	ns	3
tDPD	Min. DPD duration		500	-	500	-	500	-	us	
tDPDp	Min. period between DPD		500	-	500	-	500	-	us	
tXDPD	DPD CS# low to SCLK setup time		150	-	150	-	150	-	us	
tXPDPD	DPD Exit CS# low pulse width		200	-	200	-	200	-	ns	

Notes:

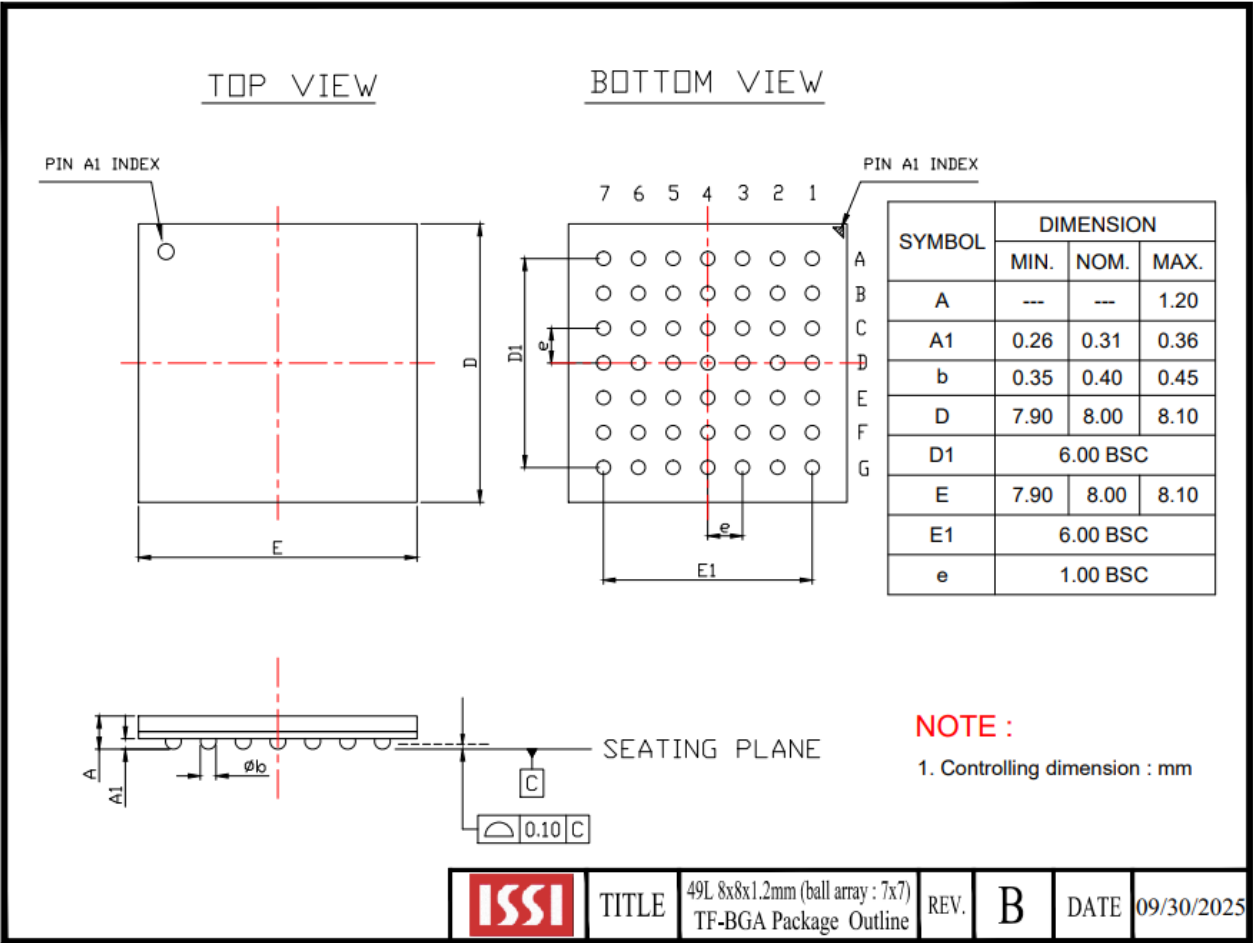
- 1) Max $0.75 * t_{CLK}$
- 2) Excluding Hybrid Sleep Exit
- 3) Maximum time is tCEM

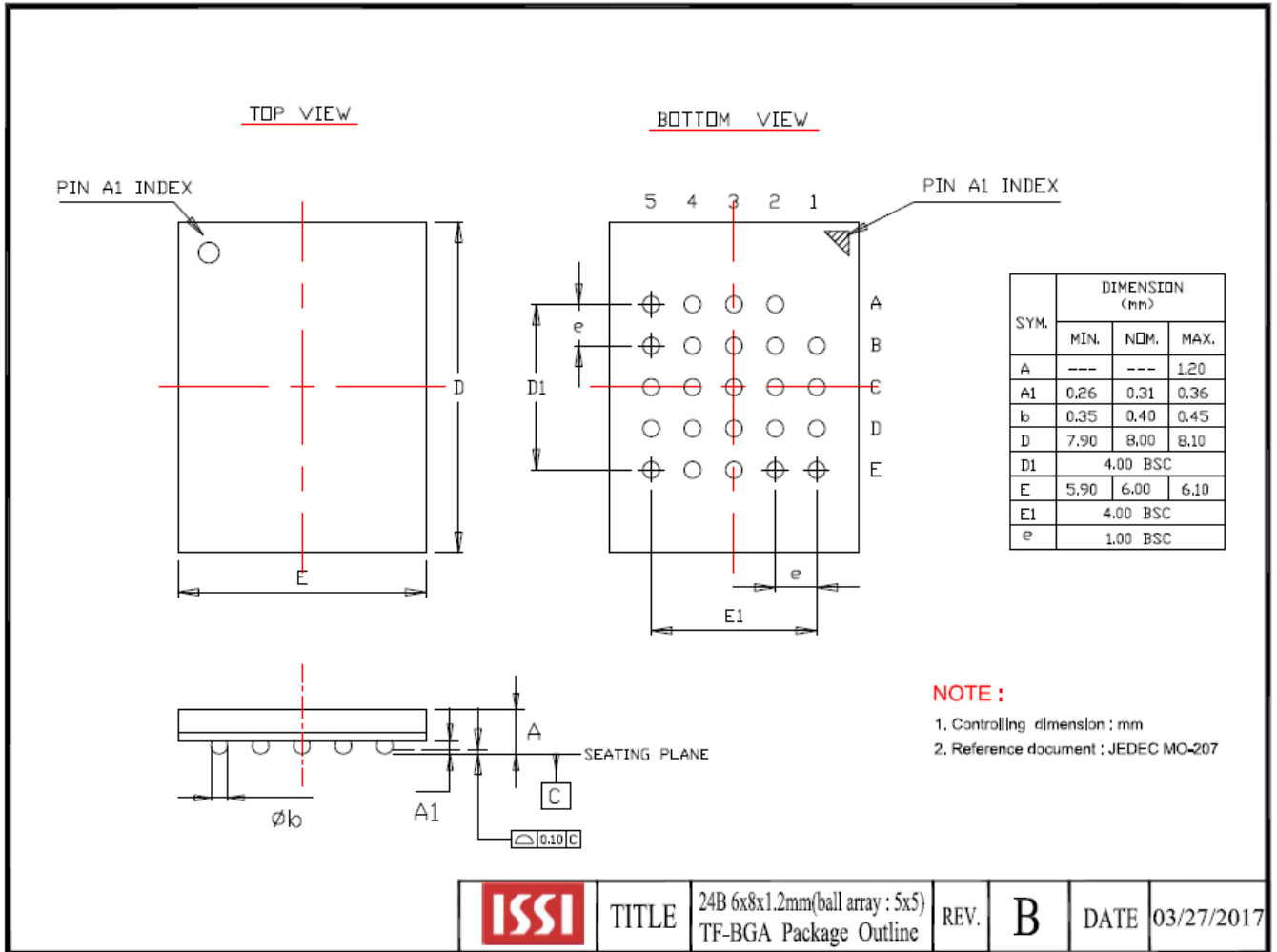
Table 8.1: READ/WRITE Timing Parameters (Continued)

Symbol	Parameter	133MHz		166MHz		200MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
tPU	Device initialization	150	-	150	-	150	-	us	
tRST	Reset# to CMD valid	2	-	2	-	2	-	us	
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from SCLK	2	6.5	2	6.5	2	6.5	ns	
tDQSQ	Skew between DQ and DQS	-	0.6	-	0.5	-	0.4	ns	
tDS	DQ and DM input setup time	0.8	-	0.6	-	0.5	-	ns	
tDH	DQ and DM input hold time	0.8	-	0.6	-	0.5	-	ns	

9. PACKAGE TYPE INFORMATION

9.1 49-BALL THIN PROFILE FINE PITCH BGA 8x8mm 7x7 BALL ARRAY (A)



9.2 24-BALL THIN PROFILE FINE PITCH BGA 6x8mm 5x5 BALL ARRAY (B)


9. ORDERING INFORMATION – Valid Part Numbers

IS66 WVX 32M16 E ALL - 200 A L I

TEMPERATURE

I = Extended (-40°C to 85°C)
A1 = Extended (-40°C to 85°C)
A2 = Extended (-40°C to 105°C)

PACKAGE CONTENT

L = Green Package (RoHS Compliant,
Halogen-Free) and TSCA Compliant

PACKAGE Type

A = 49-ball TFBGA 8x8mm 7x7 ball array
B = 24-ball TFBGA 6x8mm 5x5 ball array
W = KGD (Call Factory)

Maximum Frequency

200 = 200MHz
166 = 166MHz
133 = 133MHz (Call Factory)

VCC

ALL = 1.8V
BLL = 3.0V

Die Revision

E = die rev. E

Density/Org

32M16 = 32Mb x 16 = 512Mb

PSRAM Product Type

WVX = SPI OctalRAM

BASE PART NUMBER

IS = Integrated Silicon Solution Inc.
66 = PSRAM
67 = PSRAM for Automotive

10.0 Ordering Table

Industrial Temperature Range: (-40 °C to +85 °C)

Density	Voltage	Max. Frequency	Order Part No.	Description
32Mbx16 =512Mb	1.8V	200MHz	IS66WVX32M16EALL-200ALI	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS66WVX32M16EALL-200BLI	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS66WVX32M16EALL-166ALI	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS66WVX32M16EALL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	200MHz	IS66WVX32M16EBLL-200ALI	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS66WVX32M16EBLL-200BLI	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS66WVX32M16EBLL-166ALI	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS66WVX32M16EBLL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array

Automotive A1 Temperature Range: (-40 °C to +85 °C)

Density	Voltage	Max. Frequency	Order Part No.	Description
32Mbx16 =512Mb	1.8V	200MHz	IS67WVX32M16EALL-200ALA1	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS67WVX32M16EALL-200BLA1	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS67WVX32M16EALL-166ALA1	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS67WVX32M16EALL-166BLA1	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	200MHz	IS67WVX32M16EBLL-200ALA1	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS67WVX32M16EBLL-200BLA1	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS67WVX32M16EBLL-166ALA1	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS67WVX32M16EBLL-166BLA1	24-ball TFBGA 6x8mm 5x5 ball array

Automotive A2 Temperature Range: (-40 °C to +105 °C)

Density	Voltage	Max. Frequency	Order Part No.	Description
32Mbx16 =512Mb	1.8V	200MHz	IS67WVX32M16EALL-200ALA2	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS67WVX32M16EALL-200BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS67WVX32M16EALL-166ALA2	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS67WVX32M16EALL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	200MHz	IS67WVX32M16EBLL-200ALA2	49-ball TFBGA 8x8mm 7x7 ball array
		200MHz	IS67WVX32M16EBLL-200BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		166MHz	IS67WVX32M16EBLL-166ALA2	49-ball TFBGA 8x8mm 7x7 ball array
		166MHz	IS67WVX32M16EBLL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array