



xSPI Flash and HyperRAM MCP CONCEPT DATA SHEET

200MHz/166 (1.8V), 133MHz (3.0V), 24-Ball 5x5 array TFBGA
A2 Grade: -40°C to +105°C (200MHz/133MHz)
A3 Grade: -40°C to +125°C (166MHz/133MHz)

IS71/72WVH16M8AWO256

IS71/72WVH16M8BLO256

IS71/72WVH16M8AWO512

IS71/72WVH16M8BLO512

IS71/72WVH32M8AWO256

IS71/72WVH32M8BLO256

IS71/72WVH32M8AWO512

IS71/72WVH32M8BLO512

128/256Mb HyperRAM and 256/512Mb xSPI Flash

ADVANCED INFORMATION

FEATURES

• MCP Features

- 128/256Mb HyperRAM (PSRAM)
- 256/512Mb xSPI Flash
- Temp Grades:
Auto. A2 : -40°C to +105°C
Auto. A3 : -40°C to +125°C^(1, 2)
- Package:
6mm x 8mm 24-ball 5x5 array TFBGA

• xSPI Flash Features

- 256/512Mb xSPI Flash
- JEDEC standard xSPI interface
- Supports Standard SPI(1-1-1), Multi- I/O SPI(1-8-8/1-1-8), Octal (8-8-8) Interface
- Low Signal Counts :11 Signal pins (S#, C, DQS, DQ0~DQ7)+ optional W#, ERR#
- Double Transfer Rate (DTR) Operation
200MHz (400MB/s) at 1.8V VCC
133MHz (266MB/s) at 3.0V VCC
- In-Band, Software & Hardware Reset
- Address Parity Check function supported
- Program Array Data CRC function supported.
- Data Learning Pattern for training operation
- Dedicated W#
- Chip Erase with Uniform: Sector/Block Erase (4/32/128 Kbyte)
- More than 100,000 erase/program cycles
- More than 20-year data retention

• HyperRAM Features

- 128/256Mb HyperRAM with hidden Refresh
- HyperBUS Protocol
- 3V I/O, 11 bus signals (CK only)
- 1.8V I/O, 12 bus signals (CK, CK#)
- Double Transfer Rate (DTR) Operation
200MHz (400MB/s) at 1.8V VCC ⁽²⁾
200MHz (400MB/s) at 3.0V VCC ⁽²⁾
- Read-Write Data Strobe (DQS):
Bidirectional Data Strobe / Mask
- Configurable Latency for Read/Write Operation)
- Supports Variable Latency mode and Fixed Latency mode
- Configurable Wrapped Burst Length :
16, 32, 64, and 128
- Linear Burst Operation
- Hybrid Burst Operation

Notes: 1. xSPI Flash + 128Mb HyperRAM only.
2. HyperRAM speed is 166MHz at 125°C.



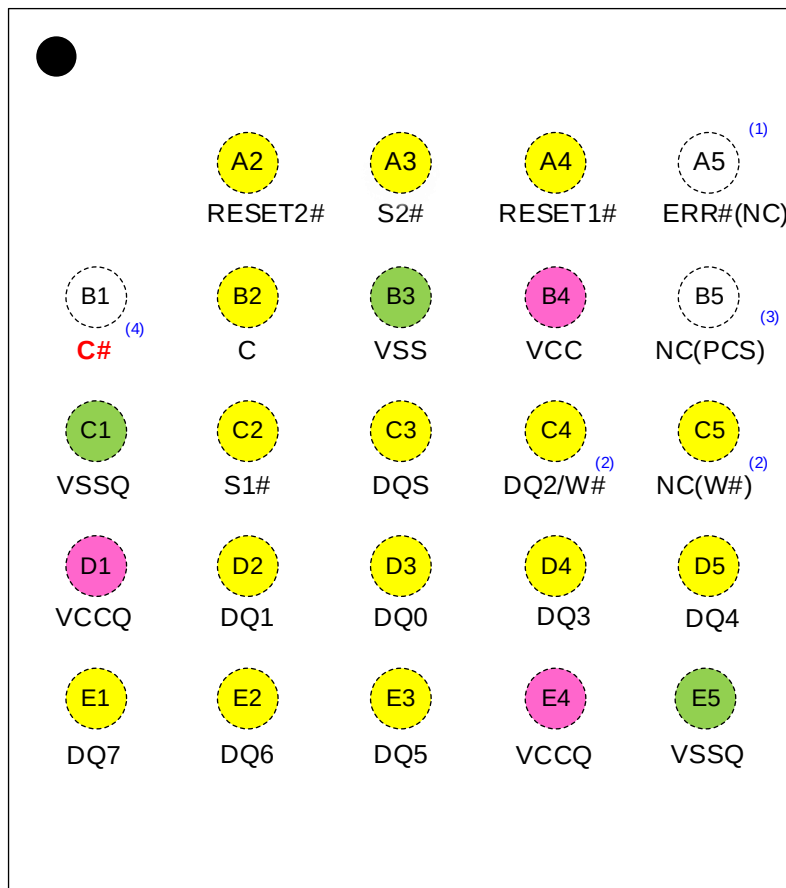
GENERAL DESCRIPTION

This document contains MCP devices for IS71/72WVH16M8AWO256, IS71/72WVH16M8BLO256, IS71/72WVH16M8AWO512, IS71/72WVH16M8BLO512, IS71/72WVH32M8AWO256, IS71/72WVH32M8BLO256, IS71/72WVH32M8AWO512, IS71/72WVH32M8BLO512

Each device is comprised of 128/256Mb HyperRAM (PSRAM) and 256/512Mb xSPI Flash.
For detailed specifications, please refer to the discrete datasheet linked below.

Document	Available at
IS66/67WVH16M8DALL/BLL Datasheet (HyperRAM)	Contact ISSI MKT
IS66/67WVH32M8DALL/BLL Datasheet(HyperRAM)	Contact ISSI MKT
IS25LX/WX256 Datasheet(xSPI Flash)	Contact ISSI MKT
IS25LX/WX512MA Datasheet(xSPI Flash)	Contact ISSI MKT

1. PIN CONFIGURATION



Notes:

1. A5 ball is an ERR# output signal for xSPI Flash (Default). Call Factory for NC instead of ERR#.
2. C5 is an NC (Default). Call Factory for Dedicated W# instead of NC on C5 ball. When W# is on C5, C4 ball will be DQ2 only.
3. B5 ball is an NC (Default). Call Factory for PSC instead of NC for xSPI Flash.
4. C#(B1) can be left floating for single ended clock, even for 1.8V device.

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
C	INPUT	Single Ended Clock: Command, address, or data information is input or output with respect to the edges of the C.
C, C#	INPUT	Differential Clock: Command, address, or data information is input or output with respect to the crossing of C/C# pair, only for HyperRAM.
S1#	INPUT	Chip Select for Flash: The Chip select (S1#) pin enables and disables the Flash device operation.
S2#	INPUT	Chip Select for HyperRAM: The Chip select (S2#) pin enables and disables the HyperRAM device operation.
RESET1#	INPUT	RESET#: Hardware RESET for xSPI Flash. There is an internal pull-up.
RESET2#	INPUT	RESET#: Hardware RESET for HyperRAM. There is an internal pull-up.
(W#)	INPUT	Optional Dedicated Write Protect for xSPI Flash: This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not be executed.
(PSC)	INPUT	Optional Phase Shifted Clock for xSPI Flash: Optional 2 nd clock to offset DQS signal from main clock (C). PSC feature is available in Octal DDR mode only.
DQ[1:0], DQ[7:3]	INPUT/ OUTPUT	Serial IO: Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as an input for command. But address and data transfer on DQ [7:0] depends on the command. Input (address, write data) can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Output data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In Octal DDR protocol, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C.
DQ[2]/W#	INPUT/ OUTPUT, Input	Serial IO2 for HyperRAM and xSPI Flash, or Write Protect for xSPI Flash: W# for Flash will be valid in SPI mode only, and will not be valid in Octal DDR mode.
DQS	OUTPUT	Data Strobe Signal for Flash: Indicates output data valid and is required to support high speed data output. Not required in extended-SPI protocol except to achieve high frequency for specific DDR commands. Used for READ but not for WRITE operations in Flash. Configured by nonvolatile and volatile configuration register bit 5 at address 00h. When enabled, DQS is driven to ground at S1# LOW and until the device is driving output data, in which case DQS toggles to synchronize data output. When not enabled, DQS is not driven. Data Strobe Signal for HyperRAM: Refresh Collision Indicator, Data Strobe Signal in Read operation, and Write Data Mask in Write operation for HyperRAM. It enabled or disabled by S2#.
ERR#	OUTPUT	Error Indication signal for xSPI Flash: Indicates ECC Event occurrence. Open Drain. External Pull-Up is required when using ERR# signal. Call Factory for NC.

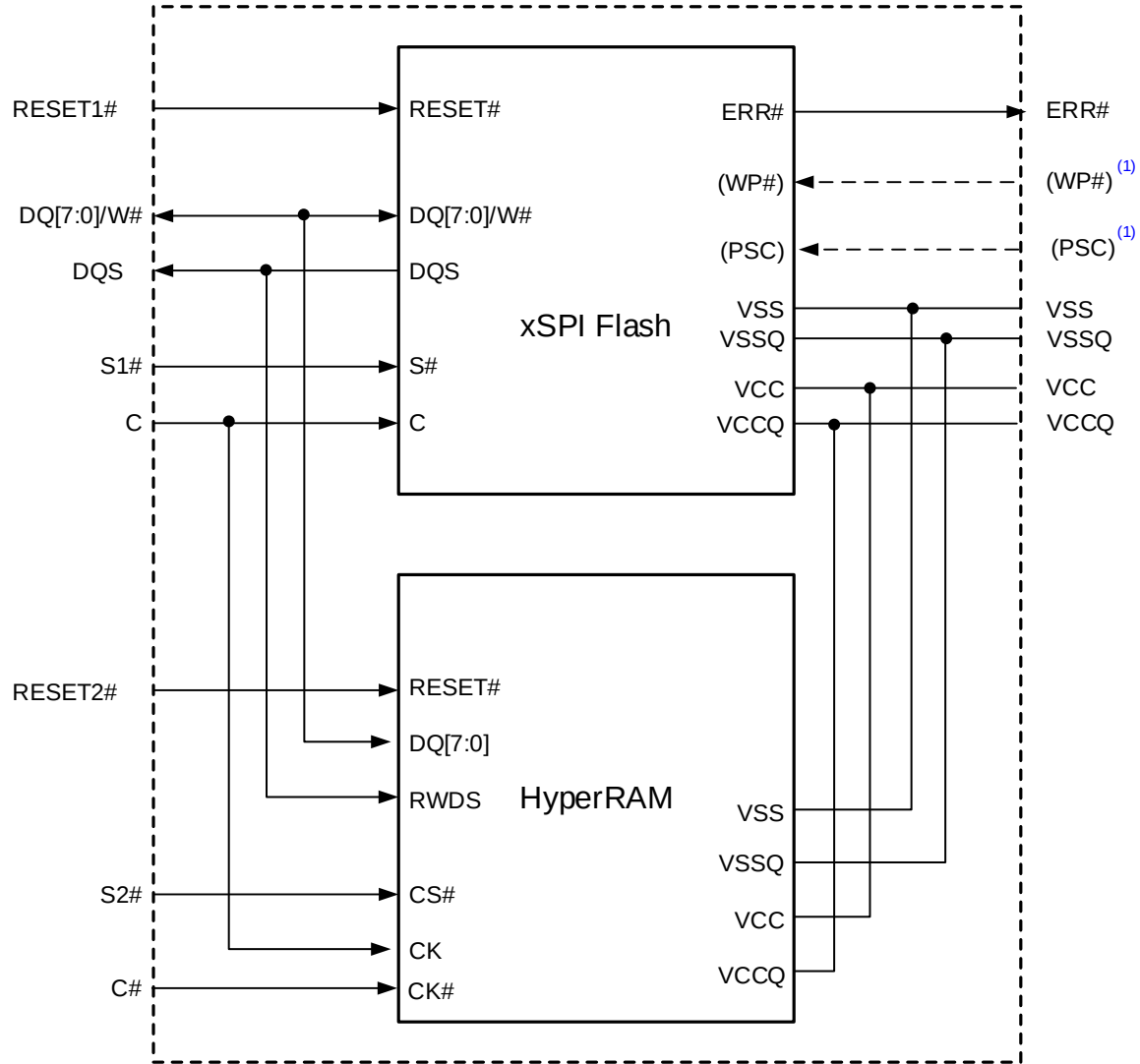
Note:

1. The MCP can work at Single Ended Clock only (C only) for 1.8V and 3.0V device.



SYMBOL	TYPE	DESCRIPTION
VCC	SUPPLY	Core Supply voltage
VCCQ	SUPPLY	DQ Supply voltage
VSS	GROUND	Core Ground: Vss is the reference for the VCC supply voltage.
VSSQ	GROUND	DQ Ground

3. BLOCK DIAGRAM



Note:

2. Dedicated WP#, PSC are optional function. Call Factory for Dedicated WP# or PSC function.



4. ORDERING INFORMATION- Valid Part Numbers

IS72 WVH 16M8 A WO 256 - 200 H L A3

TEMPERATURE RANGE

A2 = Automotive Grade (-40°C to +105°C)

A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT

L = RoHS compliant

PACKAGE Type

H = 24-ball 5x5 array TFBGA

MCP Speed

200 = 200MHz

166 = 166MHz

133 = 133MHz

Flash Density

256 = 256Mb

512 = 512Mb

Flash Type & Voltage

WO = xSPI FLASH, 1.8V

LO = xSPI FLASH, 3.0V

HyperRAM Voltage

A = 1.8V

B = 3.0V

HyperRAM Density & Org.

16M8 = 16Mb x8 (128Mb)

32M8 = 32Mb x8 (256Mb)

DRAM Family

WVH = HyperRAM (PSRAM)

BASE PART NUMBER

IS71/72 = Integrated Silicon Solution Inc.

71 = DRAM + SPI Flash MCP (Industrial Grade)

72 = DRAM + SPI Flash MCP (Automotive Grade)



IS71/72WVH16/32M8AWO/BLO256/512

Automotive (A2) Range: –40°C to +105°C

Speed Grade	Ordering Part No.	Organization	Package
-200	IS72WVH16M8AWO256-200HLA2	1.8V 128Mb HyperRAM + 1.8V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH32M8AWO256-200HLA2	1.8V 256Mb HyperRAM + 1.8V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH32M8AWO512-200HLA2	1.8V 256Mb HyperRAM + 1.8V 512Mb xSPI Flash	24-ball TFBGA. Lead free
-133	IS72WVH16M8BLO256-133HLA2	3.0V 128Mb HyperRAM + 3.0V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH32M8BLO256-133HLA2	3.0V 256Mb HyperRAM + 3.0V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH16M8BLO512-133HLA2	3.0V 256Mb HyperRAM + 3.0V 512Mb xSPI Flash	24-ball TFBGA. Lead free

Automotive (A3) Range: –40°C to +125°C

Speed Grade	Ordering Part No.	Organization	Package
-166	IS72WVH16M8AWO256-166HLA3	1.8V 128Mb HyperRAM + 1.8V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH16M8AWO512-166HLA3	1.8V 128Mb HyperRAM + 1.8V 512Mb xSPI Flash	24-ball TFBGA. Lead free
-133	IS72WVH16M8BLO256-133HLA3	3.0V 128Mb HyperRAM + 3.0V 256Mb xSPI Flash	24-ball TFBGA. Lead free
	IS72WVH16M8BLO512-133HLA3	3.0V 128Mb HyperRAM + 3.0V 512Mb xSPI Flash	24-ball TFBGA. Lead free

5. PACKAGE DRAWINGS

24-Ball Thin Profile Fine Pitch BGA 6x8mm 5x5 BALL ARRAY (H)

