Long-term Support
World Class Quality

Quality & Reliability

March 2023 Rev. E

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Quality and Reliability

At ISSI Quality and Reliability are key to our success, and of the highest priority.

ISSI Quality Systems have evolved over the years to support the company business strategy of long term support.

The ISSI Quality and Reliability Organization has team members positioned around the world to better support our customers.

ISSI Quality and Environmental Management Systems are ISO certified. While ISSI does not directly manufacture products, and therefore not eligible for automotive standard certification, the subcontractors who build products for ISSI are automotive standard certified.

ISSI's Quality Assurance Processes apply to all stages of activity. This means that Project Approval, Design and Development, Production, and Testing through Shipping are carried out in compliance to high quality standards.

Additionally, ISSI employs Quality Tools and implements the 8D process of Problem Solving for Customer Complaints in order to continually improve customer satisfaction. For product and process changes, notifications are sent out to customer via our PCN process.

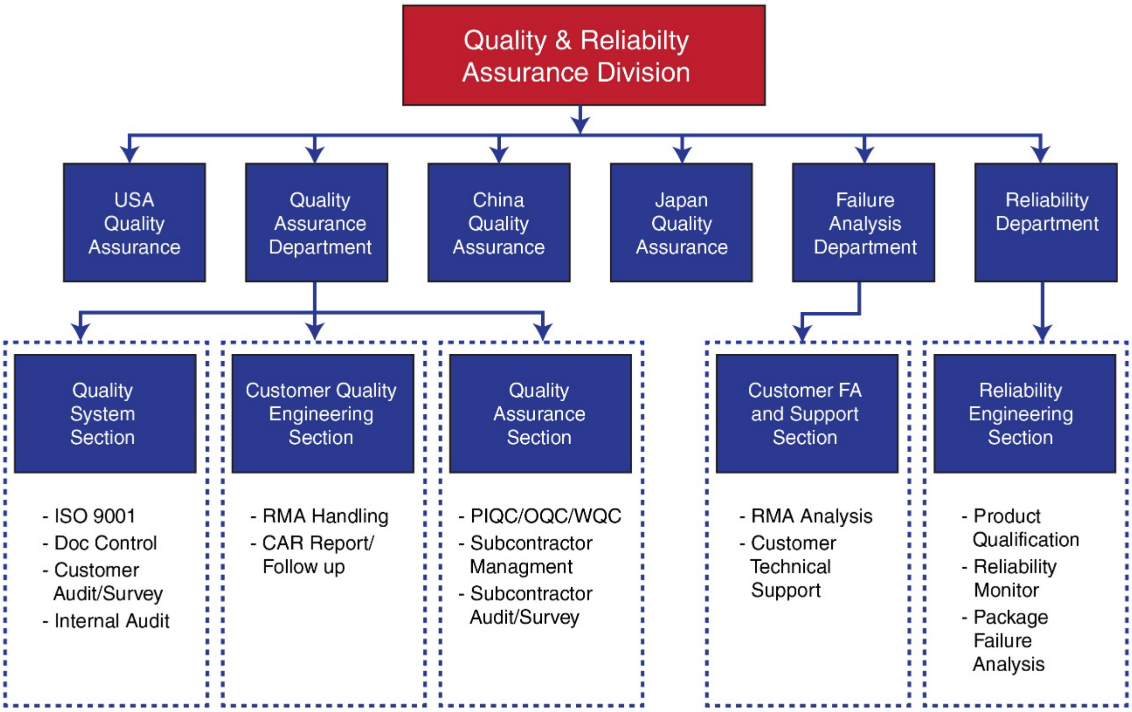
Outsourcing to our manufacturing partners is essential to our success. Consequently, the subcontractors are regarded as extensions of ISSI’s production process, particularly due to the fact that ISSI is a fabless company. ISSI's Supplier Management contributes to our strategic objectives.

Quality and Reliability Organization

ISSI headquarters is located at 1623 Buckeye Drive, Milpitas, California, USA where the corporate policies and programs are determined and applied to world-wide operations. The Taiwan facility is located in the Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C. The China office is located in Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai and in Software Park, Xiamen. The Israel office is located in Tel-Aviv 69710, handling Sales and Marketing, Design and Development of Connectivity devices

Operations in Taiwan and China consist primarily of research and development activities and

Foundry and Subcontractor management. Subcontracted operations include Wafer Fabrication, Assembly and Final Test. Many of these subcontractors are located in Taiwan and China and are managed by the Taiwan and China quality organization.



ISSI Management and all other team members are committed to:

- Understand and satisfy interested parties' expectations
- Provide defect-free products and outstanding service cost effectively
- Continuously improve ours and our partner's methods and processes
- Training that enables us to do things right
- Be the best in class in everything we do

CERTIFICATE

This is to certify that

Integrated Silicon Solution (Cayman), Inc. Taiwan Branch
Integrated Silicon Solution, Inc. (ISSI)
Chingis Technology Corp.

No. 2, Technology Road, V Hsinchu Science Park
Hsinchu
Taiwan

with the organizational units/sites as listed in the annex

has implemented and maintains a **Quality Management System.**

Scope:
The design of integrated circuits.
The management of outsourced integrated circuit production activities.

Through an audit, documented in a report, it was verified that the management system fulfills the requirements of the following standard:

ISO 9001 : 2015

Certificate registration no.	20001373 QM15
Date of revision	2021-10-15
Date of certification	2020-10-23
Valid until	2023-10-22

DQS Inc.

Brad McGuire

Brad McGuire
Managing Director

Accredited Body: DQS Inc., 1500 McConnor Parkway, Suite 400, Schaumburg, IL 60173 USA
Administrative Office: DQS Taiwan Inc., 8F, 23, Yuan Huan West Road, Feng Yuan Dist.,
Taichung City, Taiwan 420

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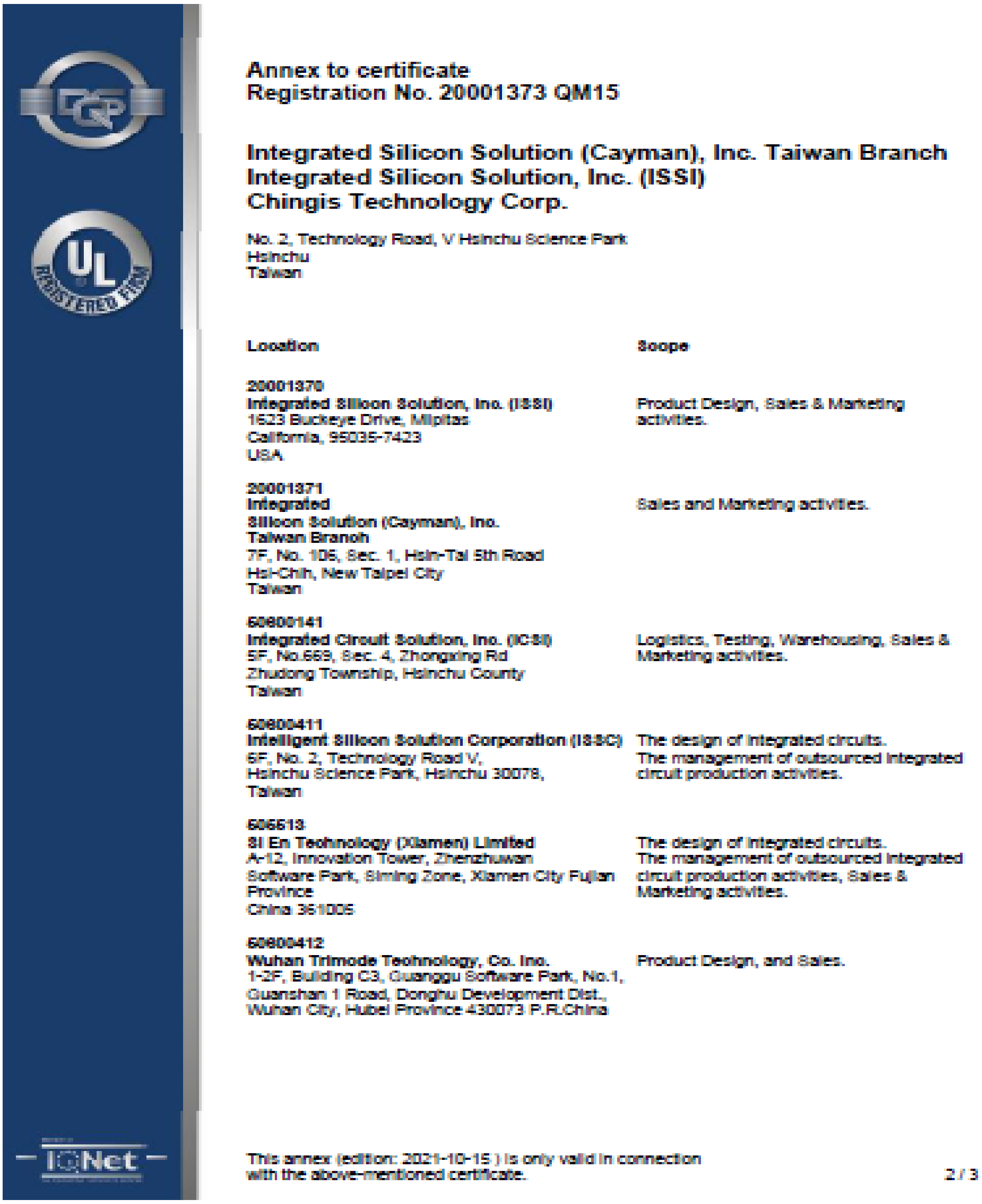

Annex to certificate
Registration No. 20001373 QM15

Integrated Silicon Solution (Cayman), Inc. Taiwan Branch
Integrated Silicon Solution, Inc. (ISSI)
Chingis Technology Corp.

No. 2, Technology Road, V Hsinchu Science Park
Hsinchu
Taiwan

Location	Scope
20001370 **Integrated Silicon Solution, Inc. (ISSI)** 1623 Buckeye Drive, Milpitas California, 95035-7423 USA	Product Design, Sales & Marketing activities.
20001371 **Integrated** **Silicon Solution (Cayman), Inc.** **Taiwan Branch** 7F, No. 106, Sec. 1, Hsin-Tai 5th Road Hsi-Chih, New Taipei City Taiwan	Sales and Marketing activities.
60800141 **Integrated Circuit Solution, Inc. (ICSI)** 5F, No.669, Sec. 4, Zhongxing Rd Zhudong Township, Hsinchu County Taiwan	Logistics, Testing, Warehousing, Sales & Marketing activities.
60800411 **Intelligent Silicon Solution Corporation (ISSC)** 6F, No. 2, Technology Road V, Hsinchu Science Park, Hsinchu 30078, Taiwan	The design of integrated circuits. The management of outsourced integrated circuit production activities.
606513 **SI En Technology (Xiamen) Limited** A-12, Innovation Tower, Zhenzhuwan Software Park, Siming Zone, Xiamen City Fujian Province China 361005	The design of integrated circuits. The management of outsourced integrated circuit production activities, Sales & Marketing activities.
60800412 **Wuhan Trimode Technology, Co. Inc.** 1-2F, Building C3, Guanggu Software Park, No.1, Guanshan 1 Road, Donghu Development Dist., Wuhan City, Hubei Province 430073 P.R.China	Product Design, and Sales.

This annex (edition: 2021-10-15) is only valid in connection
with the above-mentioned certificate.

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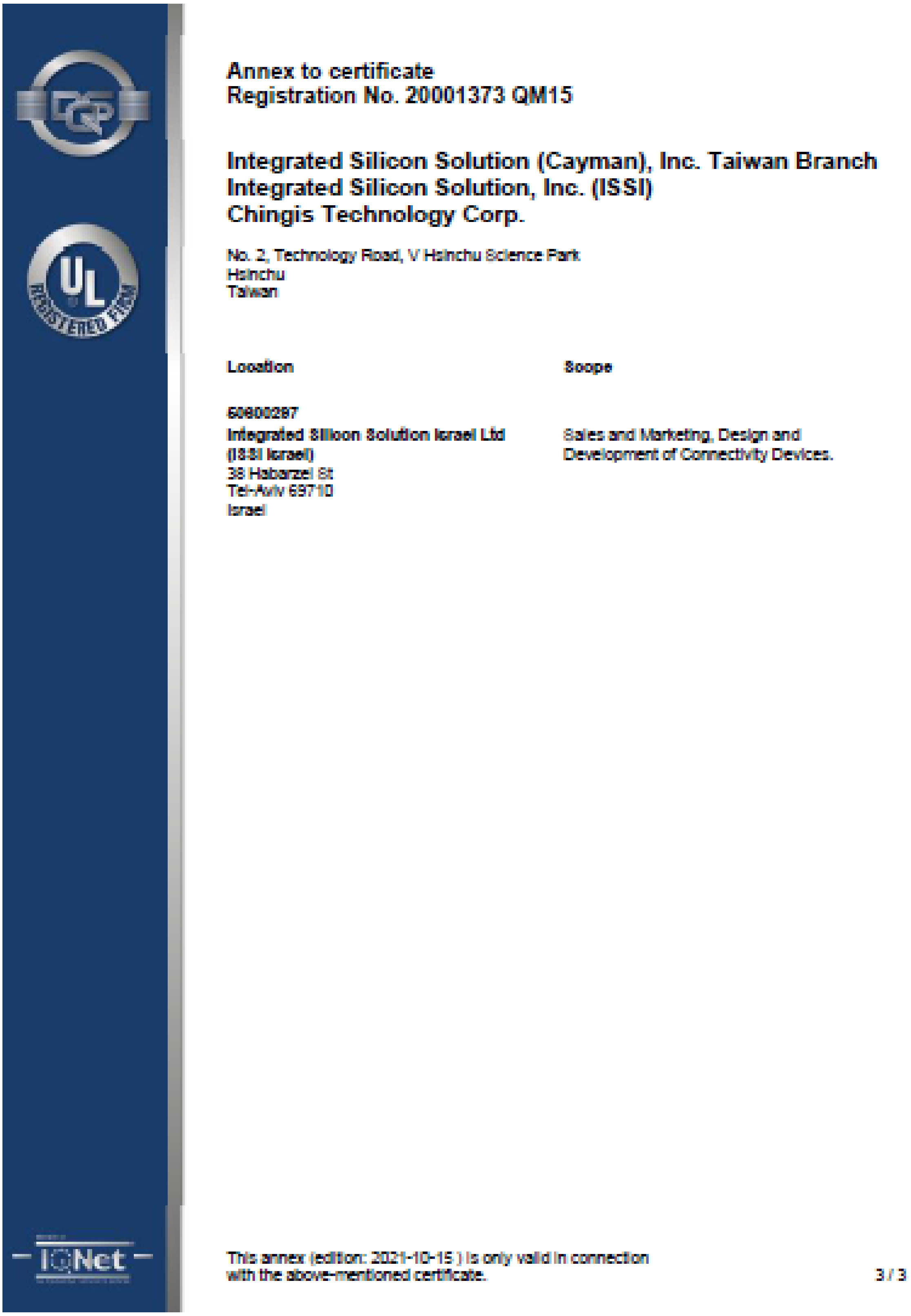

Annex to certificate
Registration No. 20001373 QM15

Integrated Silicon Solution (Cayman), Inc. Taiwan Branch
Integrated Silicon Solution, Inc. (ISSI)
Chingis Technology Corp.

No. 2, Technology Road, V Hsinchu Science Park
Hsinchu
Taiwan

Location	**Scope**
60800287 **Integrated Silicon Solution Israel Ltd** **(ISSI Israel)** 38 Habarzel St Tel-Aviv 69710 Israel	Sales and Marketing, Design and Development of Connectivity Devices.

This annex (edition: 2021-10-15) is only valid in connection
with the above-mentioned certificate.

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Figure 1-1 ISO9001 Quality System Certificate

Quality Systems

ISSI Quality systems have evolved to comply to automotive standard IATF 16949 compliance. While not all ISSI products are shipped to automotive, the system requirements have been embraced to attain more robust quality processes.

1. ISO 9001 Year 2015 Revision

The Management team has defined the quality policy and objectives for ISSI and has established a quality management system to ensure that the quality policy and quality objectives are understood, implemented and maintained. The Quality System defined in ISSI Quality Manual is in compliance with the requirements of ISO 9001: 2015. It is stratified and compiled into documents with the Quality Manuals at the top supported by procedures, specifications, regulations, rules and detailed work instructions, etc (see Figure 1-2).

Employees are trained and keep records of duties carried out according to the prescribed methods based on the latest documents to ensure that the constructed quality system is implemented in the prescribed manner.

The quality system is periodically checked and evaluated through the internal quality audits and external audits by ISO certified agencies to provide opportunities for continuous improvement.

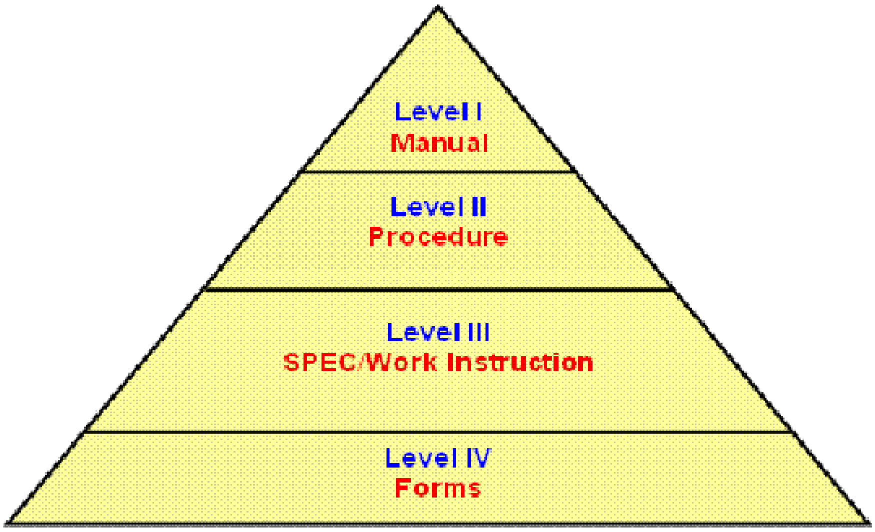


Figure 1-2 Quality Document System

ISSI in USA was certified to ISO 9001:1994 in Sept 1995. With the continuous effort in quality improvement, ISSI achieved the ISO 9001: 2000 standard in July 2002. And, ISSI is certified to ISO 9001:2008 in 2009. All ISSI locations passed ISO9001 assessments in 2005 conducted by UL (Underwriters Laboratories) current DQS one of the leading international certification bodies, as shown by the certificate issued in Figure 1-1. Since the ISO9001:2015 has been published in Sep 2015, ISSI is compliant with new revision as well as planned schedule.

ISSI is not only certified to ISO/9001 but also achieved the required quality system level as required by IATF16949 through team effort in the past few years. ISSI has implemented IATF16949 quality system requirements and has successfully passed several automotive customer audits that are leaders in the international automotive industry. All employees are moving forward through continuous improvement. As for VDA 6.3, ISSI is on the way to comply with the standard.

2. Process Map

The inter-relationship of ISSI systems is shown in the Fig 1-3.

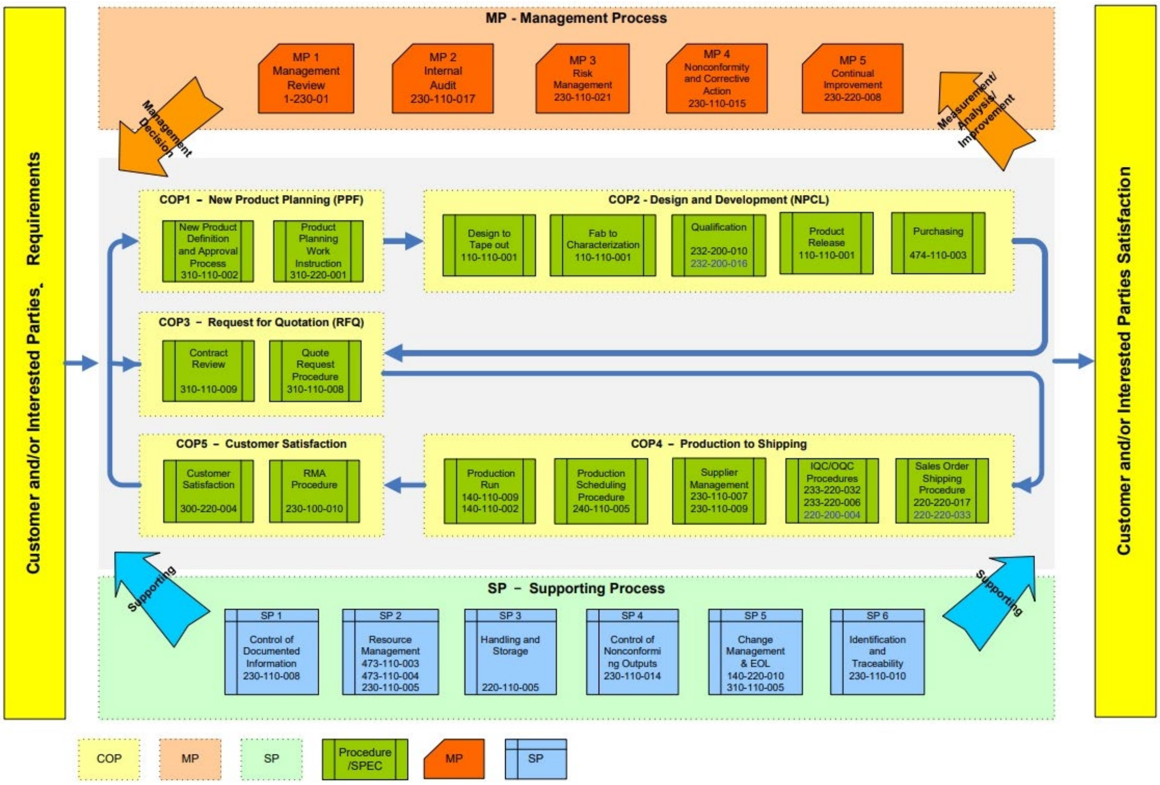


Fig 1-3 Process Map – Interaction Diagram

. Advanced Product Quality Planning

ISSI linked together the requirements of the automotive Advanced Product Quality Planning by setting up Product Planning Form (PPF) and New Project Checklist (NPCL) System. The system is web based and can be accessed by all the team members. In the NPCL system, all the steps and requirements for the life of a product can be documented and tracked. The following processes contribute to the success of the NPCL

1) Product planning – Marketing gets the new project approved

2) New Product Plan – Marketing endorses the project to Design who will work with Marketing, Development and Engineering to put the product plan together.
The consideration of Automotive Functional Safety is required at this stage. Either customer DIA or SEooC will be discussed and decided.

3) Design and Development – at this stage, Design works with Technology Development for the actual Design of the product taking into consideration customer requirements for the product. One tool used at this stage is the Design FMEA. FMEAs are discussed in the succeeding section.

4) Process Development – it is at this stage that Design and Technology Development work with Product Engineering, Assembly Engineering and QRA to develop the Production Design and Product Flow. It is also at this point that the requirements for qualifying the product are planned to verify if the actual performance of the product meets the intended characteristics. At this stage, additional tools are identified such as Production flows, Control Plans and Statistical Methods for controlling the characteristics of the product. It is also at this stage that the tool Product Part Approval Process is utilized.

5) Product Verification – the plans for verifying the conformance of the product to required characteristics is executed

6) Prototypes – ISSI also builds product prototypes which are a limited quantity of risk builds are produced as needed. During these builds the conditions and controls are the same as actual production. At this point, preliminary PpK are already computed and studied.

7) After the successful production of risk builds, then the product is ready for SLP (safe Launch Plan), when SLP is completed, then full production and ramp up. Samples for customer qualification have already passed and customers have already given feedback to ISSI on the product performance in their application.

8) Any problems encountered during the steps of the NPCL requires corrective action and lessons learned are recorded. For problem solving, ISSI uses the 8Discipline (8D) method.
Any problems encountered during the life of the product will undergo this process of problem resolution.

The interrelation shown in Figure 2 represents the activities and different department’s involvement during each phase of Advanced Product Quality Planning.

Process	Sales/ Marketing	Design Engineering	Technology Development	Product Engineering	Assembly Engineering	Reliability Engineering	Testing Engineering	QA	Purchase	Production Control
Product Planning Form	1. Issue Product planning form 2. Prepare Data sheet 3. Customer DIA or SEooC	1.Resource arrangement 2. Plan/ Schedule	1.Foundry/ Technical selection	1. Resource arrangement 2. Production flow identification	1. Assembly selection 2.Resource survey	1. Reliability survey	1. Software development 2. Wafer sort/ Final test survey		1. cost survey	1. Resource survey 2. Cost analysis
New Project Check List	Kick-off Meeting and project approved									
		1. Review DFMEA 2. Design rule check 3. Tape out document 4. Design report 5. CAD check 6. Tape-out approval/ meeting 7. Review FMEDA	1. Review mask layer spec 2. review Device cross section 3. WAT spec complete 4. Process flow 5. PPAP review (PFMEA, MSA, Control plan, SPC and production flow)	1.Sample preparing stage a. Prepare Sample b. Mosaid program c. ESD/Latch up sample d. Qualification sample e. Characterization & data review 2. Risk production Stage a. CP1 yield trigger b. CP2 yield trigger c. FT yield trigger d. CP test program release e. FT test program release	1. Marking specification 2. PPAP review (PFMEA, MSA, Control plan, SPC, Production flow) 3. process stage a. lead frame preparation b. Bonding diagram c. IC marking	1. Burn-in diagram 2. HAST diagram 3. PQR report (Device) 4. PQR report (Package)	1. Test program preparation 2. Characterization program/ report 3. Review Handler/ High Fix/ Load board /change kit 4. Wafer sort program preparation 5. Probe card	Review / Monitor every process	Follow up wafer out schedule	Handle small volume/ middle volume and mass production

				f. PPK review g. Alpha / Beta site test 3. PPAP review (PFMEA, MSA, Control plan, and production flow)						
Release Meeting	Release / Start Check meeting									

Figure 2 New Project Checklist Activity Flow

The major milestones determine the status of each new product including project approval, design development, and release to production. Each of the indicated departments must approve the new product release to production based on defined objectives that include product performance and quality.

4. Failure Mode and Effects Analysis (FMEA)

FMEA is a structured procedure for identifying and minimizing effects of as many potential failure modes as possible. FMEA was formalized as a failure analysis technique in the 50s and 60s in the aerospace industry -NASA, etc. And FMEA training program was developed by FORD in 1972 and used by all big 3 U.S. automakers.

The factors contributing to spread of FMEA are rapid advancements in technology, which are forcing manufactures to develop new products more quickly to remain competitive. With less time for testing and re-design, they must achieve their reliability target the first time around. Both of foreign and domestic competition has raised customers' expectations for quality and reliability. Also, the trend toward litigation has forced manufacturers to exercise greater care in the design and manufacture of their products.

FMEA is one of quality improvement tools. It helps reduce the effects of potential failure modes associated with key product characteristics. In general, there are three applications for purpose of design, process and service FMEA. In ISSI current situation, we started FMEA in Oct 2004 by reviewing three kinds of data and experiences, QA, FA & RMA, by concentrating on abnormality case in production line, reliability issue, case of failure analysis, customer feedback study, and case of products returned. All of FMEAs focus on design and process which helps to minimize effects of failure that results from shifting in process variables, i.e., out of spec conditions, such as misplacing ball bonds, die misalignment, holes in package, burrs on lead frame, etc. It is useful for existing products or processes that are undergoing a major design change which could affect their reliability.

The FMEA addresses the following issues:

- What function(s) is the product supposed to perform?
- How could the product fail to perform that function(s)?
- What effect would the failure have on the end product and the end user?
- How severe is the effect?
- What could cause the failure?
- How likely is the cause to actually result in the failure mode?
- What is being done to prevent or detect the cause?
- How effective is this prevention or detection method?
- What is the overall risk associated with the failure mode?
- What corrective actions can be taken to eliminate the cause of failure, or to improve the prevention or detection measure, and thus reduce the risk?

Basic Steps to Develop FMEA

1) A cross function team, made up of people from all affected functions should be formed to develop an FMEA. These could be, but are not limited to, design, process, manufacturing, marketing, operators, technicians, QA, etc., having involvement early on from these areas will help ensure that all significant areas of potential failure are addressed.

2) The cross function team can draft the FMEA by determining the information indicated on the form as following:

a) potential failure mode
b) Potential effects of failure
c) Ranking of severity
d) Potential cause/mechanisms of failure
e) Ranking of occurrence
f) Current process controls
g) Ranking of detection
h) Calculate the risk priority number
i) Recommended actions
j) Countermeasures and plans
k) Responsibility & target completion date
l) Action taken

In fact, the above items are included in the FMEA format (Fig 3). Although the purpose of FMEA is not to simply complete the form, the FMEA is a tool that helps provide new insights about the product or process. The management commitment, a cross functional team that understands and supports the FMEA process and team members with as much information about the product or process as possible are basic requirements for success of FMEA implementation.

Recommended Priority for the Corrective Action Taken

1. Priority number #1 always falls on the item with the highest score of severity. (Example Sev. ≧ 9)
2. To prioritize item by top 20% of Pareto of RPN which is a product of the Severity, Occurrence and Detection numbers (SxOxD).
3. Customer’s instruction
4. Government regulations
5. Degree of easiness in implementing corrective action

Regarding the new version AIAG-VDA FMEA, ISSI have received training courses by outsourcing consultant in Oct 2020. The relevant staffs have attended the training and have started to implement it when starting new project from Jan 2021.

As reference to US/European and some Japanese car makers have reached the agreement to adopt new FMEA for their 2022 or 2023 new models. However, since the development of a new car will take about 3 years, the required dates for its IC components are actually “Today”.

ISSI intends to apply new FMEA format by following step 1-Planning and preparation, step 2-Structure analysis, step 3-Function analysis, step 4-Failure analysis, step 5-Risk analysis and step 6-Optimization. The new FMEA requests all the “Analysis” to be linked closely with each other. It is required to list all the process steps at top level. For each step, the factors of 4M1E (Man, Machine, Material, Method and Environment) need to be addressed explicitly. Then all the items have to be linked from step 2- Structure analysis all the way to step 5-Risk analysis. Please refer to new FMEA format as Fig. 3-1.

The new FMEA seems closely related to ISO-26262 concept and need to involve related departments to work together based on given applications. It is crucial that Marketing/Sales may needs to work closely with customers to provide application scenarios so that engineering team can construct FMEA accordingly.

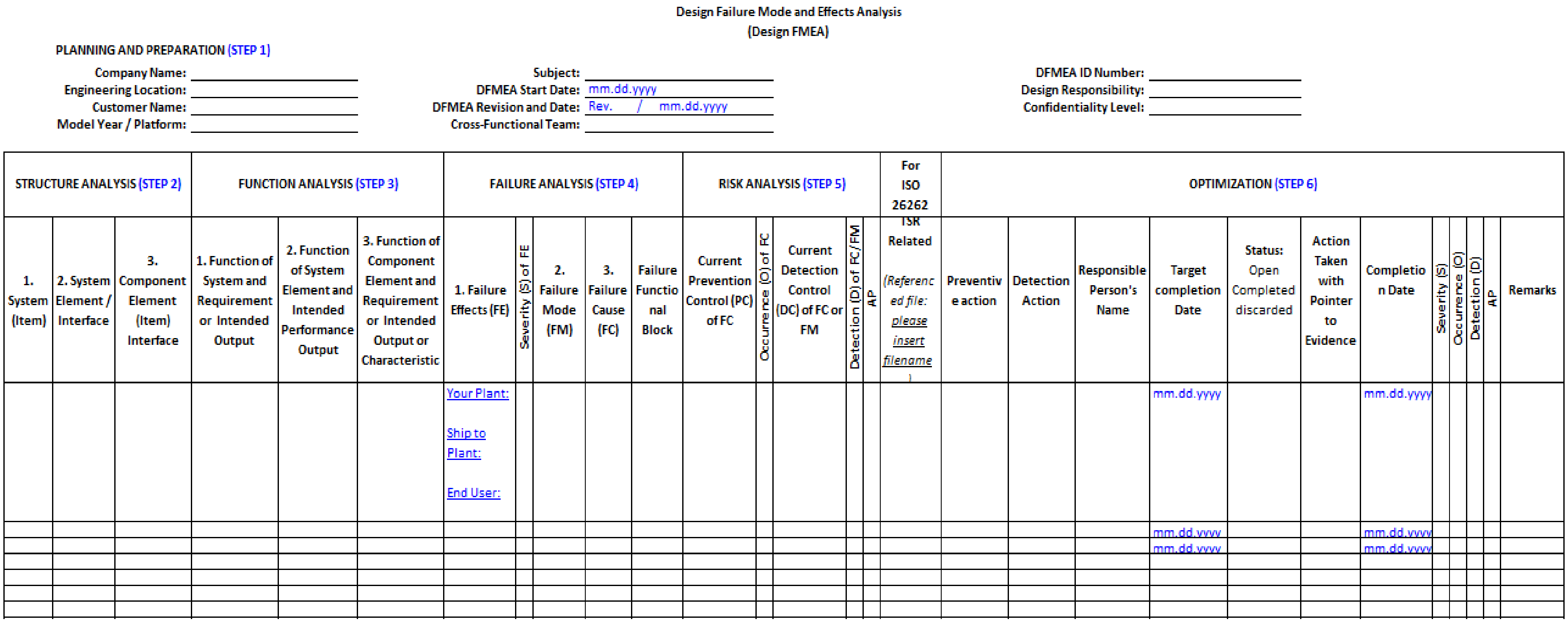
FMEA

ISSI products

S: severity, O: occurrence, D: detection, RPN: Risk Priority Number (S x O x D)

Process/ Function	Potential Failure Mode	Potential Effect(s) of Failure	Sev	Class	Potential Cause(s)/ Mechanism(s) Failure	Occur	Current Design Controls		Detect	R.P.N.	Recommended Action(s)	Responsibility & Target Completion Date	Actions Taken	Action Results			
							Prevent	Detect						Sev	Occ	Det	RPN

Fig. 3



Design Failure Mode and Effects Analysis
(Design FMEA)

PLANNING AND PREPARATION (STEP 1)

Company Name: __________
Engineering Location: __________
Customer Name: __________
Model Year / Platform: __________

Subject: __________
DFMEA Start Date: mm.dd.yyyy
DFMEA Revision and Date: Rev. / mm.dd.yyyy
Cross-Functional Team: __________

DFMEA ID Number: __________
Design Responsibility: __________
Confidentiality Level: __________

STRUCTURE ANALYSIS (STEP 2)			FUNCTION ANALYSIS (STEP 3)			FAILURE ANALYSIS (STEP 4)					RISK ANALYSIS (STEP 5)					For ISO 26262	OPTIMIZATION (STEP 6)											
1. System (Item)	2. System Element / Interface	3. Component Element (Item) Interface	1. Function of System and Requirement or Intended Output	2. Function of System Element and Intended Performance Output	3. Function of Component Element and Requirement or Intended Output or Characteristic	1. Failure Effects (FE)	Severity (S) of FE	2. Failure Mode (FM)	3. Failure Cause (FC)	Failure Functional Block	Current Prevention Control (PC) of FC	Occurence (O) of FC	Current Detection Control (DC) of FC or FM	Detection (D) of FC/FM	AP	TSR Related *(Referenced file: please insert filename)*	Preventive action	Detection Action	Responsible Person's Name	Target completion Date	Status: Open Completed discarded	Action Taken with Pointer to Evidence	Completion Date	Severity (S)	Occurrence (O)	Detection (D)	AP	Remarks
						Your Plant: Ship to Plant: End User:														mm.dd.yyyy			mm.dd.yyyy					
																				mm.dd.yyyy			mm.dd.yyyy					
																				mm.dd.yyyy			mm.dd.yyyy					

Fig. 3-1

Quality Assurance Processes

1. Quality Assurance in the Project Approval Stage

Before starting product planning, it is essential to carry out market research activities to ascertain the intended applications and the product quality/reliability demanded by each customer, and also to understand technical trends in the general marketplace, basic specifications, delivery requirements, prices, quality, reliability and other demands on products.

Information on demanded quality and reliability acquired through the above activities, various data obtained in-house from accumulated results and fundamental research on reliability technology are used to set target levels which are appropriate for product applications and operating environments and to formulate development plans.

This information is then compiled into product plans, and design specifications are drawn up based on these product plans and summarized as input for design.

1.1 Quality Assurance in the Design and Development Stage

1.1.1 Product Development and Design

Product design is an extremely important process for ensuring high quality and reliability in semiconductor devices, and it is necessary to implement both built-in quality and built-in reliability.

Product design proceeds according to the design specification. These specifications include design inputs (applicable regulations, customer demands and in-house standards) to ensure that appropriate requirements are considered. Product design goes through the stages of logic/circuit design, layout, mask design, prototype manufacture and evaluation before reaching completion.

1.1.2 Design Review

Design review consists of checking whether the design standards are the rules to be followed. Observance of design standards is checked using various simulation tools automatically or manually.

ISSI provides simulation models for each SRAM, DRAM, Flash and Analog part manufactured. These models are revised as new device and technologies are developed. Models can be obtained by contacting ISSI FAE department.

In addition, characterization data on each device are performed and retained in ISSI K2 database. These characterization data are available upon request on a case-by-case basis. Also, the Automotive Functional Safety requirement will be reviewed.

1.1.3 Product Release

The final stage before a new product is released to manufacturing is Product Release. During the final product release meeting all requirements of the NPCL are reviewed for completeness and the checklist of items for the product released are discussed. When all are supplied of the satisfaction of the team, the documentation is signed off and the product is officially released together with the qualification and characterization data to demonstrate that the product can be manufactured in accordance to requirements.

1.1.4 Production Part Approval Process (PPAP)

As part of the NPCL process, the requirements of the PPAP for automotive products are supplied whenever a product is being qualified for automotive applications.

ISSI will supply the Certificate of Design, Construction and Qualification (CoDC) as well as the Part submission Warrant (PSW) together with the various specific requirements by the automotive customer.

ISSI subcontractors (Fab and Assembly) also submit their own PPAP to ISSI for new technologies and processes.

2. Quality Assurance in the Production Stage

2.1 Wafer Processing

1) Wafer Process Technology
Since ISSI is one of the IC design leaders in the world, we serve hundreds of customers with different needs and applications. In order to satisfy all customers' needs, we offer the Memory, Logic and Analog products with leading-edge IC process technologies in 25nm, 30nm, 38nm, 40nm, 45nm, 55nm, 60nm, 63nm, 72nm, 90nm, 99nm, 0.11-micron, 0.13-micro, 0.15-micron and 0.18-micron generations as well as 0.35-micron, 0.5-micron for Analog products.

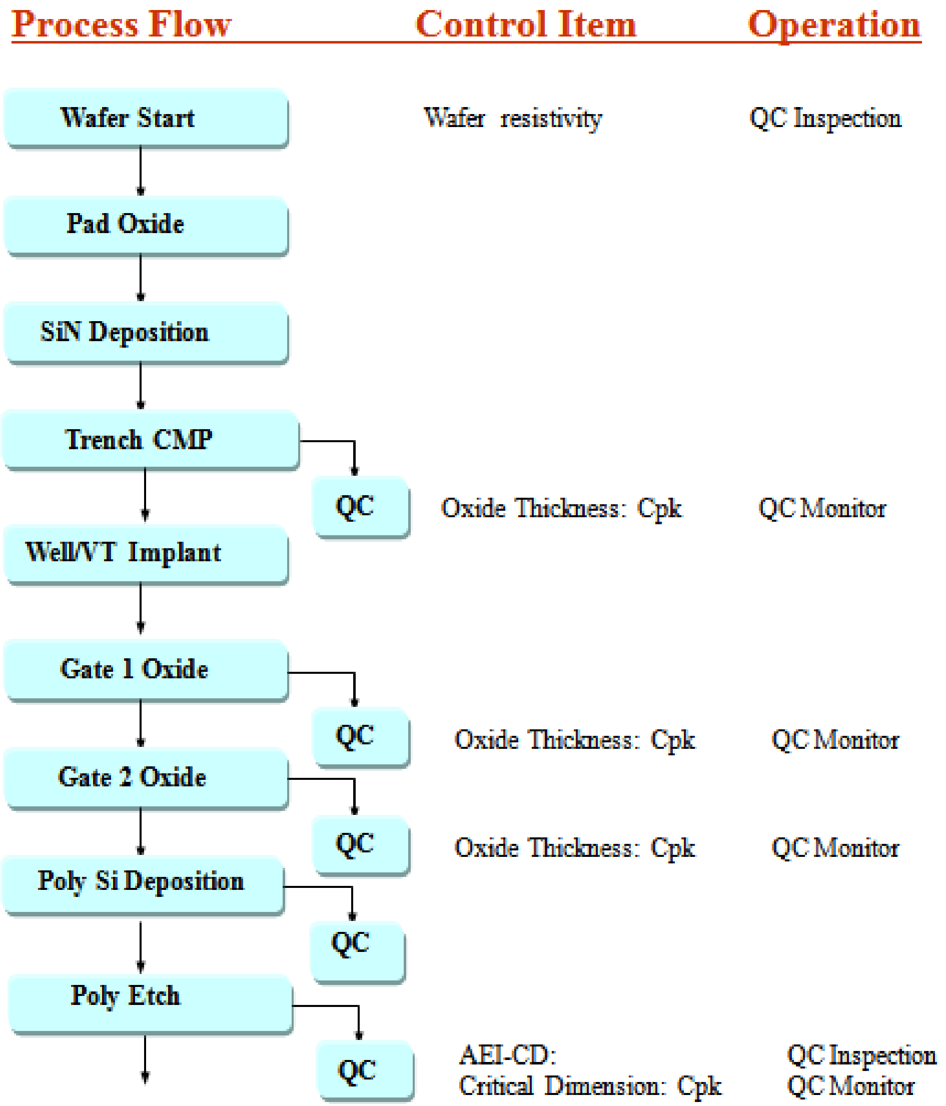
The process technology is developed in accordance with standardized methodologies. Each new technology must pass a rigorous qualification procedure based on typical industry standards before it is released to mass production.

Once in production, every released process is constantly monitored against a predetermined set of standards. The monitor results are then published in the foundry's website and ISSI QA will periodically access the database for evaluation.

Products released to production are monitored at the wafer and package level. Wafer acceptance test (WAT) data by lot indicate key process measurements tested to specified limits. Packaged units are periodically monitored for reliability based on package family and assembly line.

2) Wafer Process Flow and In-line Control

The generic wafer process flow and major control items are shown in Figure 3-2 with SRAM as an example.



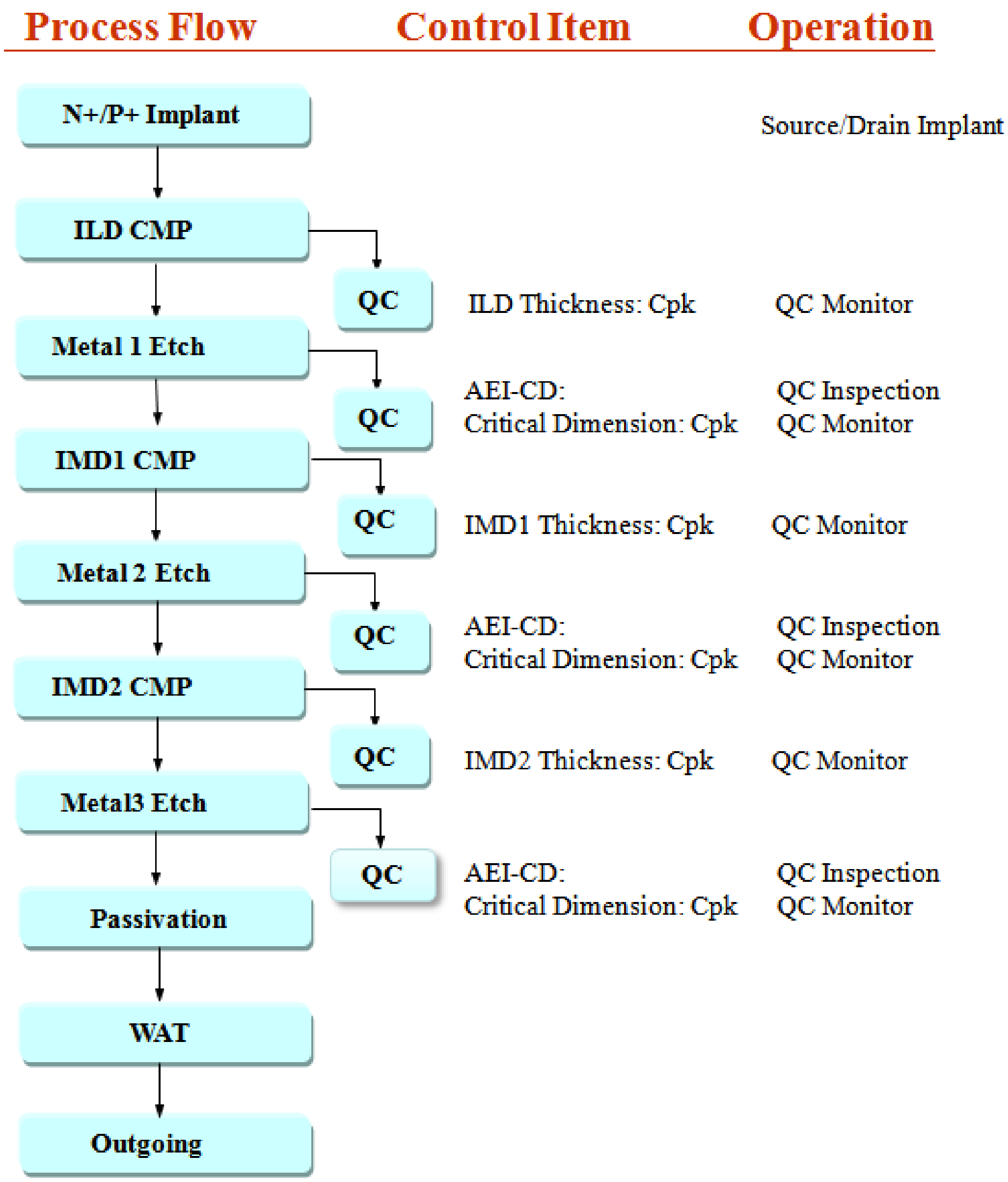
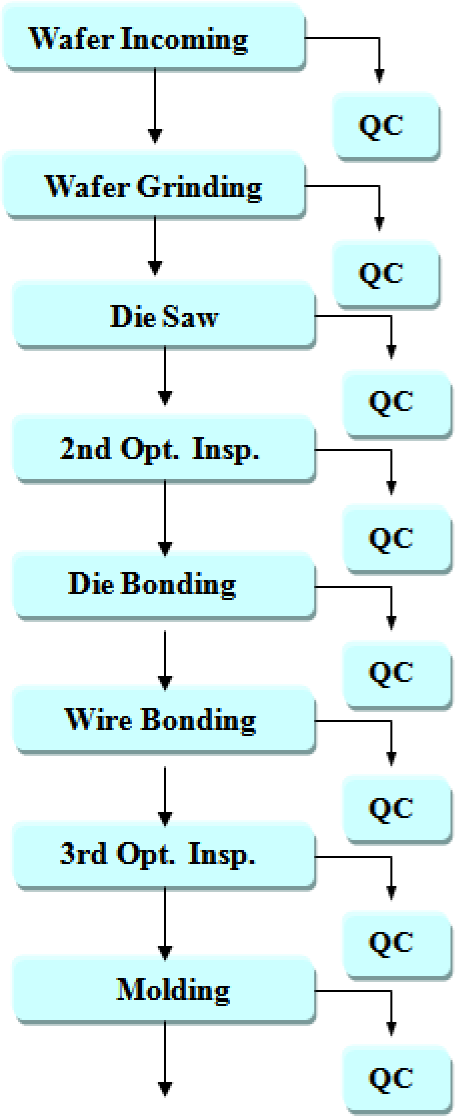


Figure 3-2 Generic SRAM Wafer Process & Control

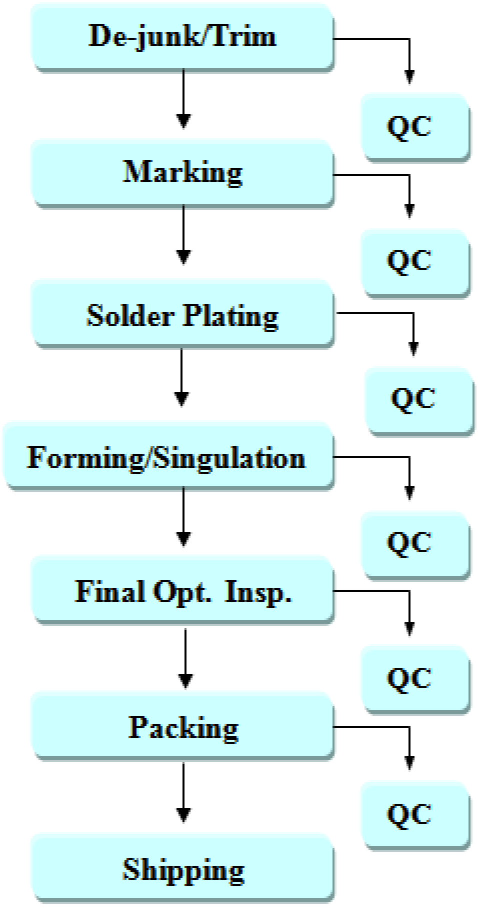
2.2 Assembly Process Technology

Our qualified assembly houses offer IC packaging design and fabricate a full array of packages for ISSI products, with pin counts from 8 to more than 365. Major packaging offers include ball grid array (PBGA, TFBGA), quad flat packages (PQFP, TQFP, LQFP), small outline packages (SOP, TSOP, SOJ), PLCC and Dual/Quad flat no-lead (DFN.QFN) for Analog products. To ensure that they create world-class packages, the major assembly houses are ISO 9000, IATF 16949 and ISO 14001 certified companies.
The generic assembly process flow and major control item are shown in Figure 3-3.

For the Automotive Functional Safety project, part of our Subcontractors including Assembly and Final testing houses are certified ISO26262 process audit by certification bodies.



Process Flow	KEY Control	Operation
Wafer Incoming → QC	Particle/Metallization	QC Inspection
Wafer Grinding → QC	Wafer Thickness	QC Monitor Cpk
Die Saw → QC	Saw Kerf Width	QC Monitor Cpk
2nd Opt. Insp. → QC	Chip Crack	QC Inspection
Die Bonding → QC	Epoxy Fillet/Void (Traditional package) Peeling testing (LOC)	QC Inspection
Wire Bonding → QC	Bond Cratering Bond Pull/ Ball Shear	QC Inspection QC Monitor Cpk
3rd Opt. Insp. → QC	Damaged Wire Broken Wire	QC Inspection
Molding → QC	Incomplete Fill/ Wire sweep Molding temperature	QC inspection QC Monitor Cpk



Process Flow	KEY Control	Operation
De-junk/Trim → QC	Dam-bar cutting burr	QC Inspection
Marking → QC	Legibility/Complete Mark	QC Inspection
Solder Plating → QC	Thickness/ Composition	QC Monitor Cpk
Forming/Singulation → QC	Package dimension Coplanarity	QC Inspection QC Monitor Cpk
Final Opt. Insp. → QC	Appearance	QC Inspection
Packing → QC	Packing/ Labeling Outgoing	QC Inspection
Shipping		

Figure 3-3 Generic Assembly Process & Control

2.3 Testing

1) Overview

The purpose of testing is to verify the conformance to ISSI specifications and/or customer requirements before the products are delivered to customers. Testing is an inspection process that is needed because the failures have not been eliminated. The failures are usually caused by design errors, materials and process defects, operational environment extremes, and aging effects.

Although testing does not add value to the product, ISSI recognizes it is crucial to recruit skilled engineering expertise to guarantee testing quality. This requires a sizable investment, however, we believe it is a necessity for any company intending to become, or remain as, a leading logic and memory supplier.

Electrical testing consists of three steps: 1) continuity test, 2) DC parametric test, and 3) functional and dynamic test (AC). It is used for verifying IC performance and conformance to ISSI published data sheet so that "bad" parts[1] are not shipped to the customers. The electrical specification limits and conditions are related to the wafer fabrication process parameters and thus to the potential physical defects that might occur.

2) SRAM/DRAM/Flash/Analog Product Testing Flow

The templates of Commercial SRAM, DRAM, Flash, Analog TEST Flow & Control are shown in Figures 3-4, 3-5, 3-6 and 3-7 respectively.

3) Known Good Die Testing Flow

In addition to the package products ISSI offers die only material to customers. Known good Die (KGD) business and service is provided to our customers upon request. The generic KGD Test Flow and Control is shown in Figure 3-8.

These die could be in wafer form. Also, the customer can choose an option of tested die without speed testing (Known Tested Die) or die that had gone through burn-in and full testing (Known Good Die)

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[1] The unit of measurement for this is typically a parts-per-million (ppm) value for the defective parts shipped to customer.

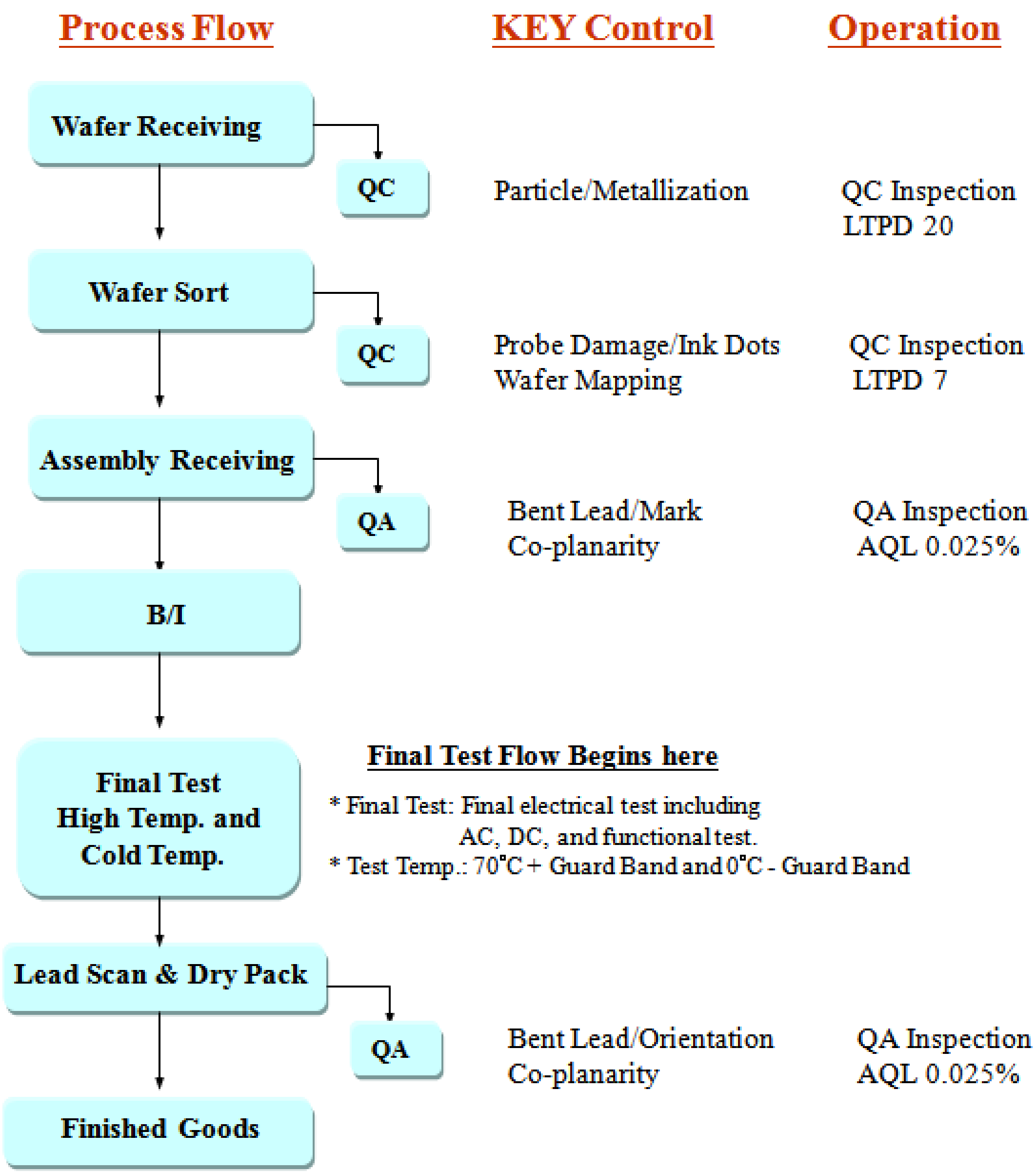


Figure 3-4 Commercial SRAM Test Flow & Control

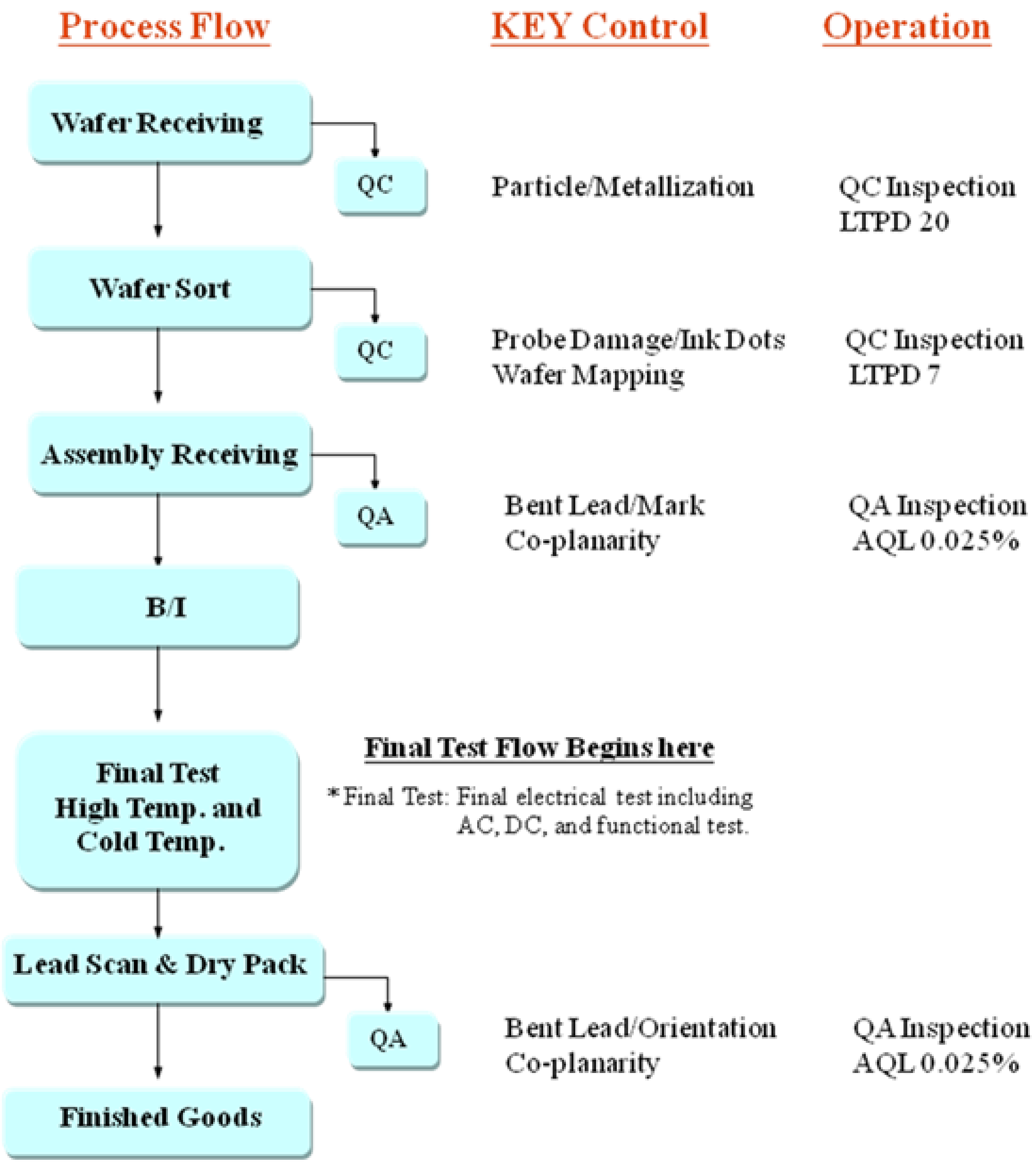


Figure 3-5 Commercial DRAM Test Flow & Control

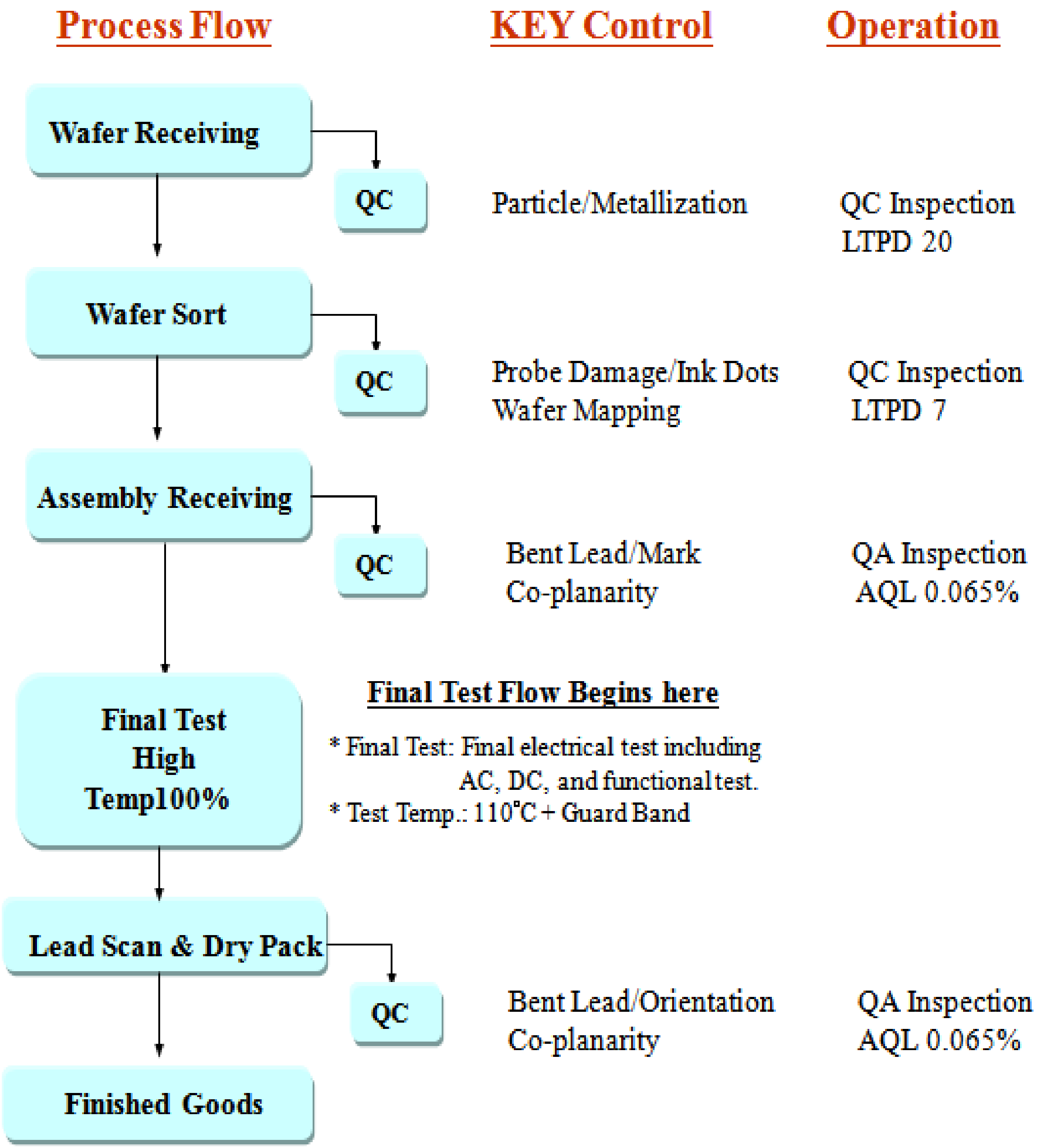
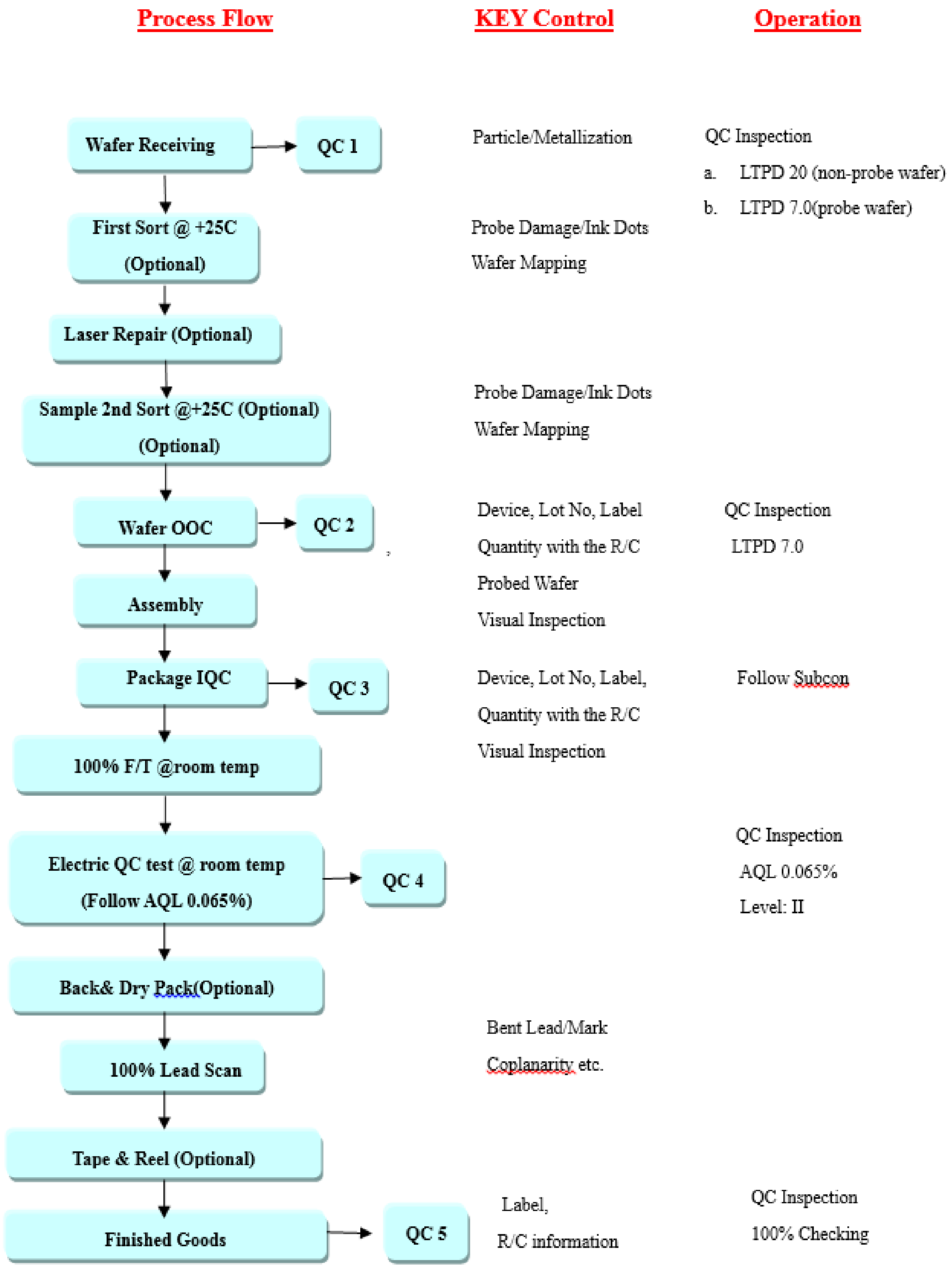


Figure 3-6 Commercial Flash Test Flow & Control



Process Flow	KEY Control	Operation
Wafer Receiving → QC 1	Particle/Metallization	QC Inspection a. LTPD 20 (non-probe wafer) b. LTPD 7.0(probe wafer)
First Sort @ +25C (Optional)	Probe Damage/Ink Dots Wafer Mapping	
Laser Repair (Optional)		
Sample 2nd Sort @+25C (Optional) (Optional)	Probe Damage/Ink Dots Wafer Mapping	
Wafer OOC → QC 2	Device, Lot No, Label Quantity with the R/C Probed Wafer Visual Inspection	QC Inspection LTPD 7.0
Assembly		
Package IQC → QC 3	Device, Lot No, Label, Quantity with the R/C Visual Inspection	Follow Subcon
100% F/T @room temp		
Electric QC test @ room temp (Follow AQL 0.065%) → QC 4		QC Inspection AQL 0.065% Level: II
Back& Dry Pack(Optional)		
100% Lead Scan	Bent Lead/Mark Coplanarity etc.	
Tape & Reel (Optional)		
Finished Goods → QC 5	Label, R/C information	QC Inspection 100% Checking

Figure 3-7 Commercial Analog Test Flow & Control

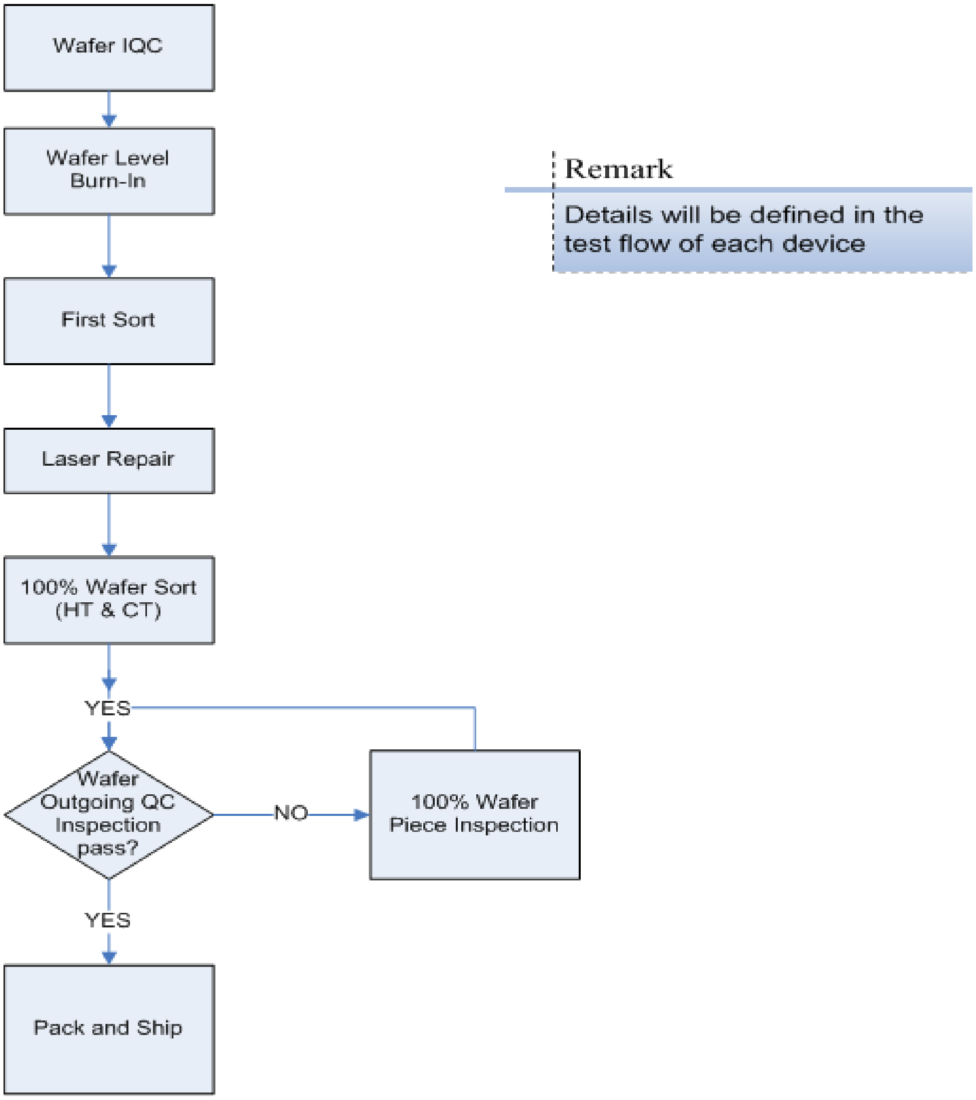


Figure 3-8 General Known Good Die Test Flow & Control

2.4 Quality Assurance of Product Shipping

Checks are carried out to ensure that the quality control established in the development and manufacturing stages is being reliably executed. Shipping inspections are performed to confirm the quality assurance of each lot in order to ensure the quality and reliability of shipped products.

The shipping inspection includes visual check and sampling of electrical characteristics. Visual check consists of checks on lead bending, marking defects, chipping, voids and defects. Electrical characteristics involve DC and AC characteristics as described in (section 2.4.1) “Monitoring Data for AOQL”.

After the final inspection, judgment is made to confirm that the electrical specifications, appearance and packing condition of shipped products satisfy the specifications demanded by customers.

2.4.1 Monitoring Data for AOQL

ISSI establishes outgoing quality level target, measurement and procedure for continuous improvement.

a) The target of outgoing quality level for ISSI products is less than 20 ppm for Memory and Analog products. This target is periodically reviewed by management representative to approach the goal of zero defects.

b) All the device types will be measured to establish the outgoing quality level. QC shall issue quality discrepancy report (QDR) for the devices that fall below the targeted quality level and require analysis improvement until the desired quality level is achieved.

c) The average outgoing quality level (AOQL) is sampled from the ISSI inventory parts, and the sample lots should be included to be tested by each testing subcontractor.

Outgoing quality levels will be published by QRA and distributed to appropriate persons.

For Analog/Logic products, there are very few devices in stock and the AOQL is not monitored at present.

Customer Complaints

1. ISSI RMA Process

Field quality information is an essential factor for improvement of product quality. Equally important are the investigation of field failures and feedback of results to the customers.

When a customer desires to return product, a return material authorization (RMA) form identifying the customer, the product, and the nature of the customer's concern should be completed. There are six types of returned material that ISSI accepts from customers. These are:

1) Administrative:

Customer received wrong parts, wrong quantity, order entry error, duplicate shipment barcode label errors, etc. Shipping discrepancies must be reported within 60 days of shipment.

2) Customer Convenience:

Customer doesn't want the parts even though they are what they ordered and work according to specification.

3) Electrical:

Parts failed to function as specified or did not work in the application.
Electrical RMAs usually require an FA.

4) Failure Analysis:

Customer has requested in depth failure analysis on returned part(s)

5) Stock Rotation:

Product returned from distributors

6) Visual/Mechanical:

Visual inspection failures such as bent leads, coplanarity, tape & reel

If the RMA involves a quality issue, a FA RMA is requested and the appropriate failure analysis engineer is immediately notified. A customer who needs to receive information on the cause of the failure can request failure analysis to be performed. Within 48 hours of ISSI QRA's receipt of the returned product, a preliminary report will be issued, to verify the customer complaint.

If the product function meets ISSI specifications, the customer will be contacted and the application will be investigated

If, on the other hand, the product proves to be defective, a failure analysis will be done to determine the cause and corrective action will be taken. Within two weeks of ISSI QRA's receipt of the returned product, the customer will receive a final report documenting the completion of the failure analysis and the cause of the failure.

2. RMA Flow Chart

ISSI has developed procedures and e-RMA system for providing and controlling returns from customers for failure and non-failure issues. See flow as shown in Figure 1 for failure issues.

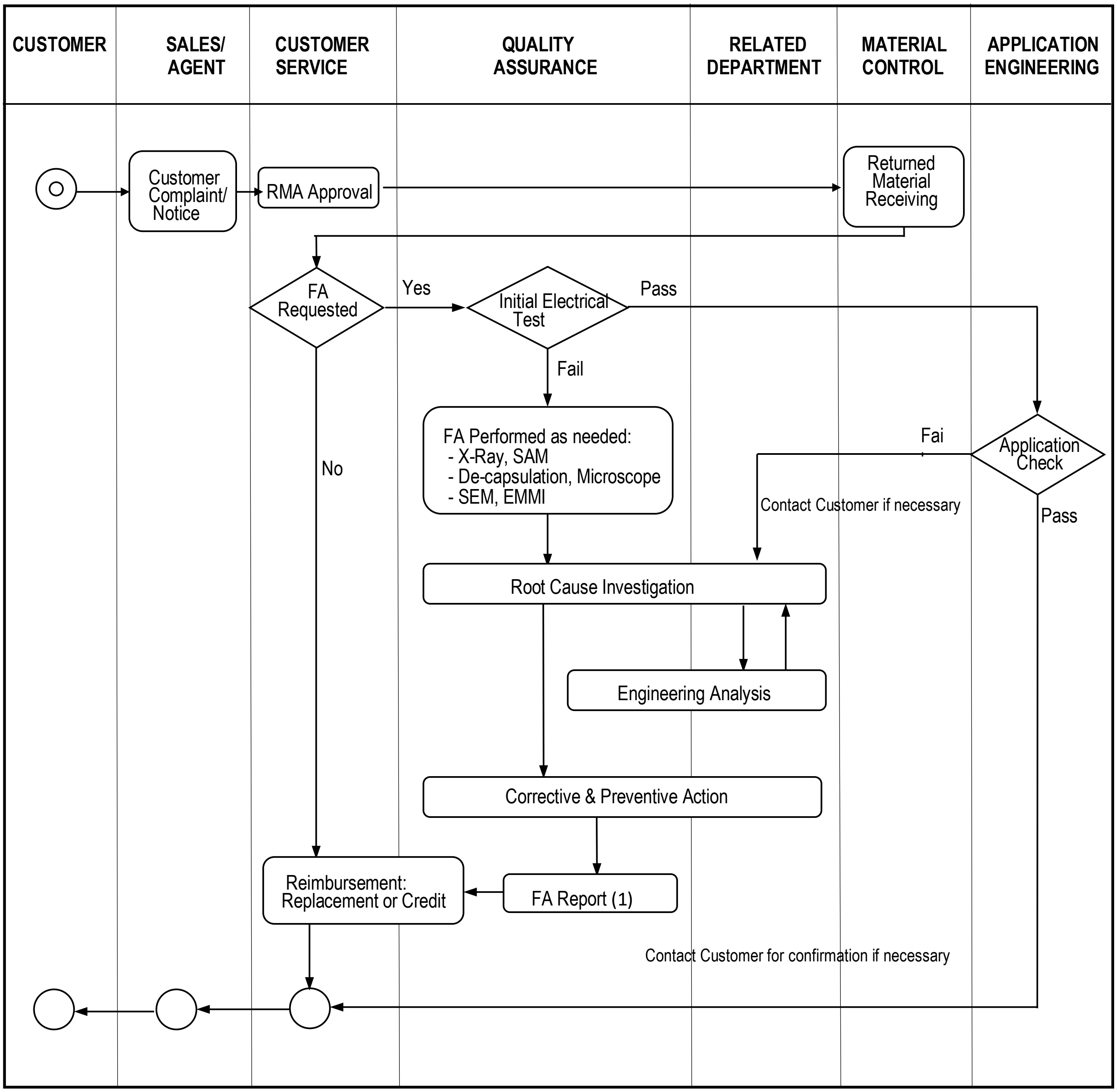


Figure 1 RMA Process Flow

3 Corrective Action

For ISSI's commitment to continuous quality improvement, a corrective action request (CAR) procedure is established according to the ISO 9001:2015 and JEDEC 671 standard. The Corrective Action methodology follows the 8 Discipline process.

ISSI shall take action to eliminate the cause of non-conformities in order to prevent recurrence. Corrective actions shall be appropriate to the effects of the non-conformities encountered. A documented procedure shall be established to define requirements for

1) reviewing non-conformities (including customer complaints),

2) determining the causes of non-conformities,

3) evaluating the need for action to ensure that non-conformities do not recur,

4) determining and implementing action needed,

5) recording the results of action taken, and

6) reviewing corrective action taken.

7.) verifying that the action taken is effective

4 Preventive Action

ISSI shall determine action to eliminate the causes of potential non-conformities in order to prevent their occurrence. Preventive actions shall be appropriate to the effects of the potential problems. A documented procedure shall be established to define requirements for

1) determining potential non-conformities and their causes,

2) evaluating the need for action to prevent occurrence of non-conformities,

3) determining and implementing action needed,

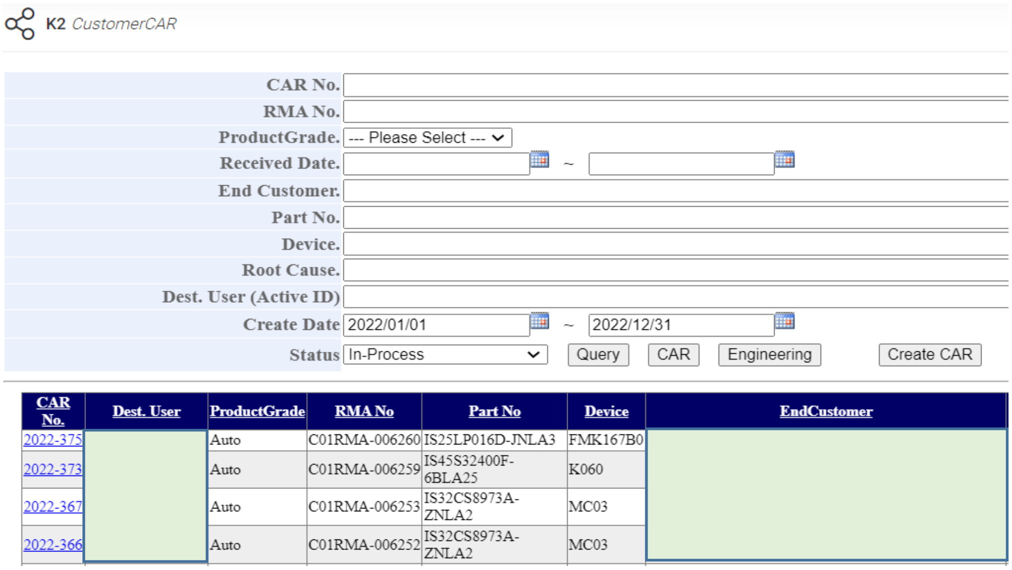
4) records of results of action taken, and

5) reviewing the preventive actions taken.

e-CAR

The electronic Corrective Action Request (e-CAR) system was established by ISSI IT and QRA on K2 Platform. The e-CAR is used to record and track the most important quality issues including in-house design and operations, customer complaint, and subcontractor's processes. The data is reported to periodic corporate meeting and quarterly management review meeting.

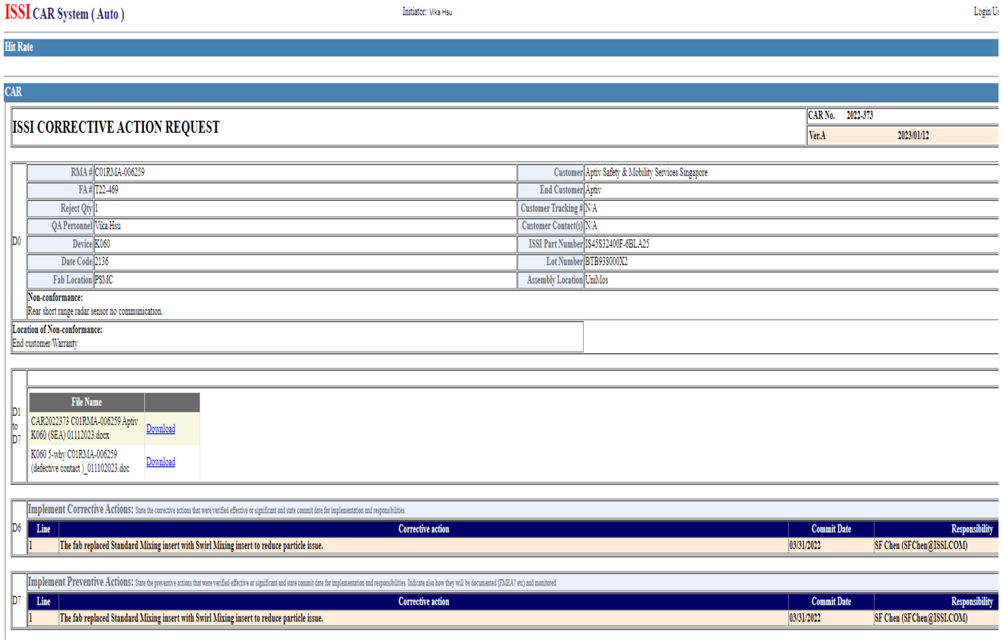
The e-CAR Report as shown in Figure 2 is a listing of the CAR's accumulated year to date. Each individual CAR is accessible electronically on the database. E-CAR can also be searched by date, processor or status. Online CAR is based on 8D method as shown in Figure 3



CAR No.	
RMA No.	
ProductGrade.	--- Please Select ---
Received Date.	~
End Customer.	
Part No.	
Device.	
Root Cause.	
Dest. User (Active ID)	
Create Date	2022/01/01 ~ 2022/12/31
Status	In-Process

CAR No.	Dest. User	ProductGrade	RMA No	Part No	Device	EndCustomer
2022-375	[redacted]	Auto	C01RMA-006260	IS25LP016D-JNLA3	FMK167B0	[redacted]
2022-373	[redacted]	Auto	C01RMA-006259	IS45S32400F-6BLA25	K060	[redacted]
2022-367	[redacted]	Auto	C01RMA-006253	IS32CS8973A-ZNLA2	MC03	[redacted]
2022-366	[redacted]	Auto	C01RMA-006252	IS32CS8973A-ZNLA2	MC03	[redacted]

Figure 2 e-CAR Report



Initiator: Vika Hsu

ISSI CORRECTIVE ACTION REQUEST

CAR No. 2022-373
Ver.A 2023/01/12

D0

RMA #	C01RMA-006259	Customer	Aptiv Safety & Mobility Services Singapore
FA #	T22-469	End Customer	Aptiv
Reject Qty	1	Customer Tracking #	N/A
QA Personnel	Vika Hsu	Customer Contact(s)	N/A
Device	K060	ISSI Part Number	IS45S32400F-6BLA25
Date Code	2136	Lot Number	BTB938000X2
Fab Location	PSMC	Assembly Location	UniMos

Non-conformance:
Rear short range radar sensor no communication.

Location of Non-conformance:
End customer/Warranty

D1 to D7

File Name	
CAR2022373 C01RMA-006259 Aptiv K060 (SEA) 01112023.docx	Download
K060 5-why C01RMA-006259 (defective contact)_011102023.doc	Download

D6 Implement Corrective Actions: State the corrective actions that were verified effective or significant and state commit date for implementation and responsibilities.

Line	Corrective action	Commit Date	Responsibility
1	The fab replaced Standard Mixing insert with Swirl Mixing insert to reduce particle issue.	03/31/2022	SF Chen (SFChen@ISSI.COM)

D7 Implement Preventive Actions: State the preventive actions that were verified effective or significant and state commit date for implementation and responsibilities. Indicate also how they will be documented (FMEA? etc) and monitored.

Line	Corrective action	Commit Date	Responsibility
1	The fab replaced Standard Mixing insert with Swirl Mixing insert to reduce particle issue.	03/31/2022	SF Chen (SFChen@ISSI.COM)

Figure 3 e-CAR Example

Change Control

Quite often, changes are made to products or manufacturing process in order to improve quality, reliability and/or productivity.

The feasibility of these changes is judged using sufficient data indicating that the change will not produce any negative effects.

When a change is planned, all related departments review the change and its potential impact. In the case of changes that have a significant effect on product, these results are conveyed in advance to customers to confirm that there is no deteriorated effect at the customer side.

After these judgments are received, if the change is acceptable, instructions are issued and initial control of floating data is performed as necessary for the final check.

The ISSI change list is shown below (Table 1) and its system flow is depicted in Figure 4.

Item	Lead Time
Die Technology	3 months
Foundry Site	3 months
Wafer Fabrication Process	3 months
Assembly House	3 months
Assembly Process	3 months
Marking	3 months
Data Sheet	3 months
Packing	3 months
Discontinue	6 months

Table 1 ISSI Change List

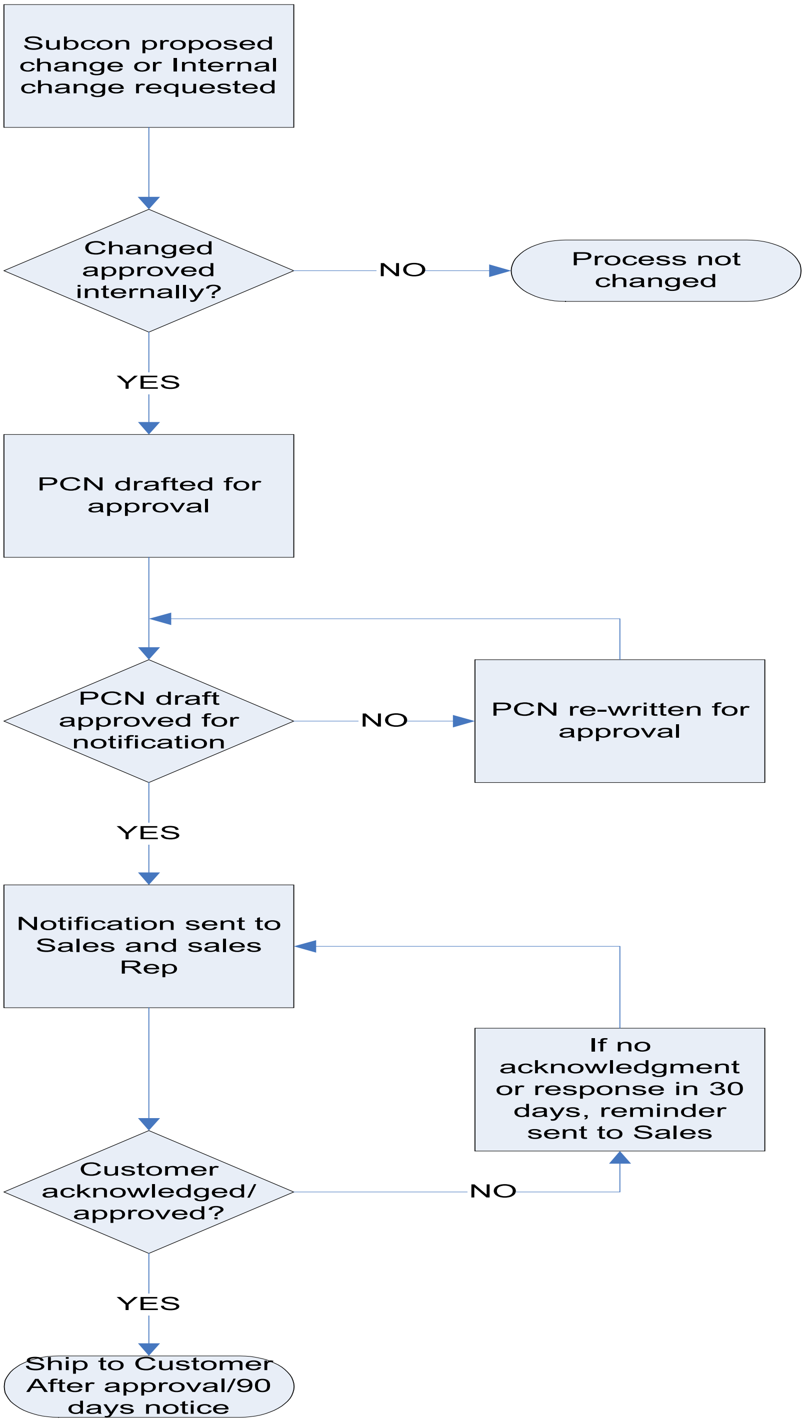


Figure 4 ISSI Change System

Management of Subcontractors

1. Task Force

On average, 40% of production cost is due to material procurement; therefore, subcontractor management is extremely important. It follows that a substantial portion of quality problems is related to the subcontractor. Establishment of a partnership is essential in order for both parties to succeed in their business.

The subcontractor should make a positive contribution to design, production, and cost reduction. Emphasis should be placed on the total material cost, which includes that of price and quality. In order to ensure high quality, ISSI QA and relevant engineering departments are performing on-site process monitoring via a task force unit as shown in Figure 1.

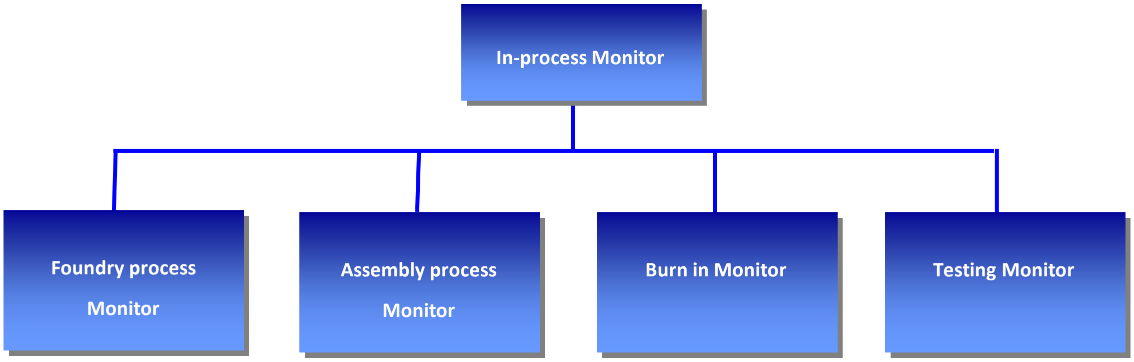


Figure 1

2. Methodology

Subcontractor management activities include:

1) Subcontractor qualification & Approved Vendor List control

2) Control of bill of material (BOM) and process

3) Package IQC

4) Monthly key process Cpk[1] (> 1.67) report

---

[1] Cpk is an index of process capability. It measures the process stability with respect to the standards over a certain period. To calculate Cpk, it is necessary to calculate another index, Cp, which measures the data bias toward the standard center.

$$C_p = \frac{(\text{upper limit} - \text{lower limit})}{6\sigma} \quad \text{and}$$

$$C_{pk} = \frac{|\text{standard limit closest to the average value - average}|}{3\sigma}$$

where σ is the standard deviation

5) Reliability monitoring (plus de-lamination, die crack, and cratering check)

6) Foundry/ Assembly/ Testing house rating

7) Monthly/ Quarterly meeting with key subcontractors

8) In-process monitor

9) Process control (Man, Machine, Material, Method)

10) Product output (inspect good and reject parts in each stage)

11) ISSI finding and reporting

12) Subcontractor's action and continuous improvement

13) Review FMEA (corrections effectiveness validation)

14) Regular and non-regular on side audit

3. Quality Rating / Audit

Subcontractor quality ratings provide an objective measurement of a subcontractor's performance. This measurement will lead to a subcontractor review, allocation of business, and identification of the areas for quality improvement. ISSI subcontractor management team conducts monthly review meeting on subcontractors' performance, product quality and relevant business. It is not only monthly review but also quarterly rating and ranking review meeting at ISSI. In order to continuously improve product quality, ISSI team informs rating and ranking to individual subcontractors in order to ask for improvement actions particularly if the rating is lower than 70%.

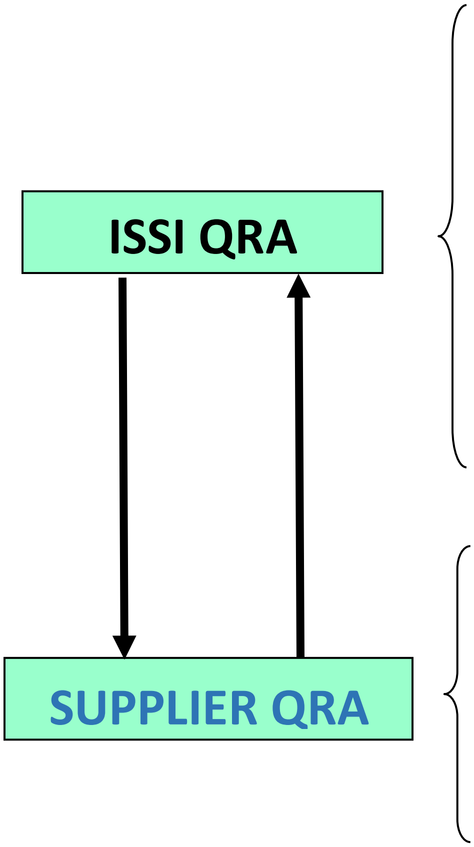
ISSI audit team is mainly composed of senior QA engineer, QS engineer and relevant PE, RE, TD, PC engineering people. QA is the leader of annual audit team when performing audit at subcontractor site. Audits are planned at beginning of every year. The annual audit schedule is the basis of the audit plan. Also, a random audit could be performed in case of anomaly or occurrence of a serious product quality problem.

The vendor quality ratings are based on certain measures and are weighted as follows:

Element	**Point Value**
1. Quality Contribution	**40**
2. Technology	**15**
3. Flexibility/ Service	**15**
4. Cost	**15**
5. Delivery	**15**

4. Supplier Relationship

Subcontractor relationship is vital to product quality. In ISSI, bi-directional communication/meetings with suppliers are periodically held to review if the supplier performance follows ISSI's requirements closely. The key communication items are defined in the following diagram (Figure 2):



ISSI QRA

- Qualifying all process and material changes
- Yearly audit arrangement for QS and process
- Yield monitoring & fail bin analysis
- Continuous improvements
- Physical/Construction Analysis for all technologies
- Reliability monitoring plan
- Monthly/Quarterly meeting with key suppliers
- Quarterly review supplier rating system
- Change Notification
- Fan-out lessoned learn & get feedback

Supplier QRA

- Moisture classification on all surface mount package types
- Packing method and material control
- AOQL data collection per week
- Critical Parameter Cp/Cpk Monthly Report
- Process FMEA/ Control plan key item identification
- Visual inspection for each lot/ shipment

Figure 2 Supplier Relationship

5. Subcontractor process control

Following the process flow, the quality control flow along with the process control plan are established for producing either mature packages or advance packages at subcontractor manufacturing process. In order to avoid potential failure, the key characteristics are linked with the living document FMEA which will be reviewed regularly.

ISSI products are manufactured following a developed process control flow and quality control flow. Also, the subcontractor QC staff monitors in-line process and product performance based on defined quality control plan and inspection/test criteria. In case of nonconforming product, subcontractor quality team follows defined procedure to dispose nonconforming product and inform ISSI QA staff if severe quality discrepancy is found.

ISSI QA team is responsible for subcontractor management. The team coordinates with subcontractor in reviewing both process stability and product quality periodically.
If any product quality discrepancy is found, corrective action or improvement action is required. The effectiveness of correction will be tracked and verified in a timely manner by ISSI QA team depending on the severity of the nonconforming event.

6. Production line ESD control/management

Electrostatic Discharge (ESD) is well known in the semiconductor industry that the IC component could be severely damaged if the ESD program is not well maintained. The ESD protection/wiring was built during the facility construction. In compliance to standard ANSI S20.20/JESD 625/JEDEC JS-001 and JS-002, ESD protection is widely applied in the production line such as personnel conductive garments, footwear, gloves, wrist strap, ESD flooring system, worktable mat, ionizer to neutralize the charge, conductive container. Also, there is an "ESD protected area" sign and a lock gate system installed at front door of ESD sensitive area.

Subcontractors including Foundry Fab, Assembly, Final testing and Packing houses have defined regular monitor schedule to check the personnel grounding and the connection of grounding of machine/working table/stock shelf and mobile push cart in the ESD sensitive area. Also, the ESD resistance is required to be measured and reviewed periodically.

ISSI QA staff is well trained on ESD related knowledge and have practical experiences in the production line. ESD protection is one of check items to be verified when ISSI QA conducts on-site audit. The ESD verification will be commenced once there is ESD damaged product suspected until the concern can be eliminated.

Functional Safety

ISO 26262 implementation

ISSI kicked-off ISO 26262 project in July 2017. A series of training courses, on site workshop exercises, SC-AFSP (Automotive Functional Safety Professional for Semiconductor) training/ certificated and process audit were completed in Nov 2018. ISSI planed starting for 1st product certification by compliance with ISO 26262 standard, one of 4G DDR products had been certificated in Apr 2021. Also, the 3rd party SGS to present the award ceremony to ISSI in achieving ISO 26262 Product Certification and published in the periodical.
ISSI requested its subcontractor to implement ISO 26262 and get process certificate in order to follow

ISSI’s strategic to meet automotive safety requirement, not only starts from product design phase but also involve product production processes of whole lifecycle.

Failure Analysis

ISSI Failure Analysis function is divided into two major categories. One is "Lab Service" and the other is "Internal Engineering Application". Customer Complaints utilize the Lab service and follow the prescribed FA flow and cycle time is measured. ISSI has continually improved the capability of the Failure Analysis Lab to meet the increasing demands of the industry.

See FA Instrument List

4.1 Establishment of Failure Analysis Laboratory

1 Electrical Failure Analysis (EFA) Laboratory

Prior to 1998 -- For the purpose of engineering debug and verification of the IC’s electrical characteristic in the wafer and package levels, MOSAID 3490 with probe station, HP 4145 (semiconductor parameter analyzer) and oscilloscope were acquired.

Early in 2000 -- In order to test high-speed and low power products in variable temperatures, MOSAID 4155 and thermal controller instrument were added.

2 Assembly Engineering and Chemical Laboratory

By the end of 1998 -- SAT (Scanning Acoustic Tomography), X-ray, package sawing machine, mechanical polishing machine, chemical hood, auto de-capping machine etc. were set up for the purpose of further quality improvement in packaging.

Early in 1999 -- Bonding wire defects, package delamination, die and passivation cracks, etc. could be detected by using these instruments and the information was quickly passed to the assembly house for improvement.

3 Physical Failure Analysis (PFA) Laboratory

Prior to 1999 -- PFA was performed mostly in the US based parent company, ISSI.

In 2000 -- Not only for engineering debugs but also for customer service, portable EMMI (Emission Microscope), FESEM (Field Emission Scanning Electron Microscope) equipped with

EDS (Energy Dispersive Spectroscope), RIE (Reactive Ion Etching) and wire bonding system were set up sequentially to improve the PFA capability.

Early in 2001 -- ISSI FA laboratory became fully capable of performing FA works, from electrical analysis to physical failure analysis. Defects, such as gate oxide damage, via abnormality, metal damages, etc., induced during production line or field application can be detected. This FA capability helps reducing the cycle time from the product’s development stage to its mature stage, improving the production yield and expediting the customer service.

4.2 Failure Analysis Function

The failure analysis function can be divided into two major categories. One is “Lab Service Items ” and the other is “Internal Engineering Application”. The detailed contents are listed in Figure 4-1.

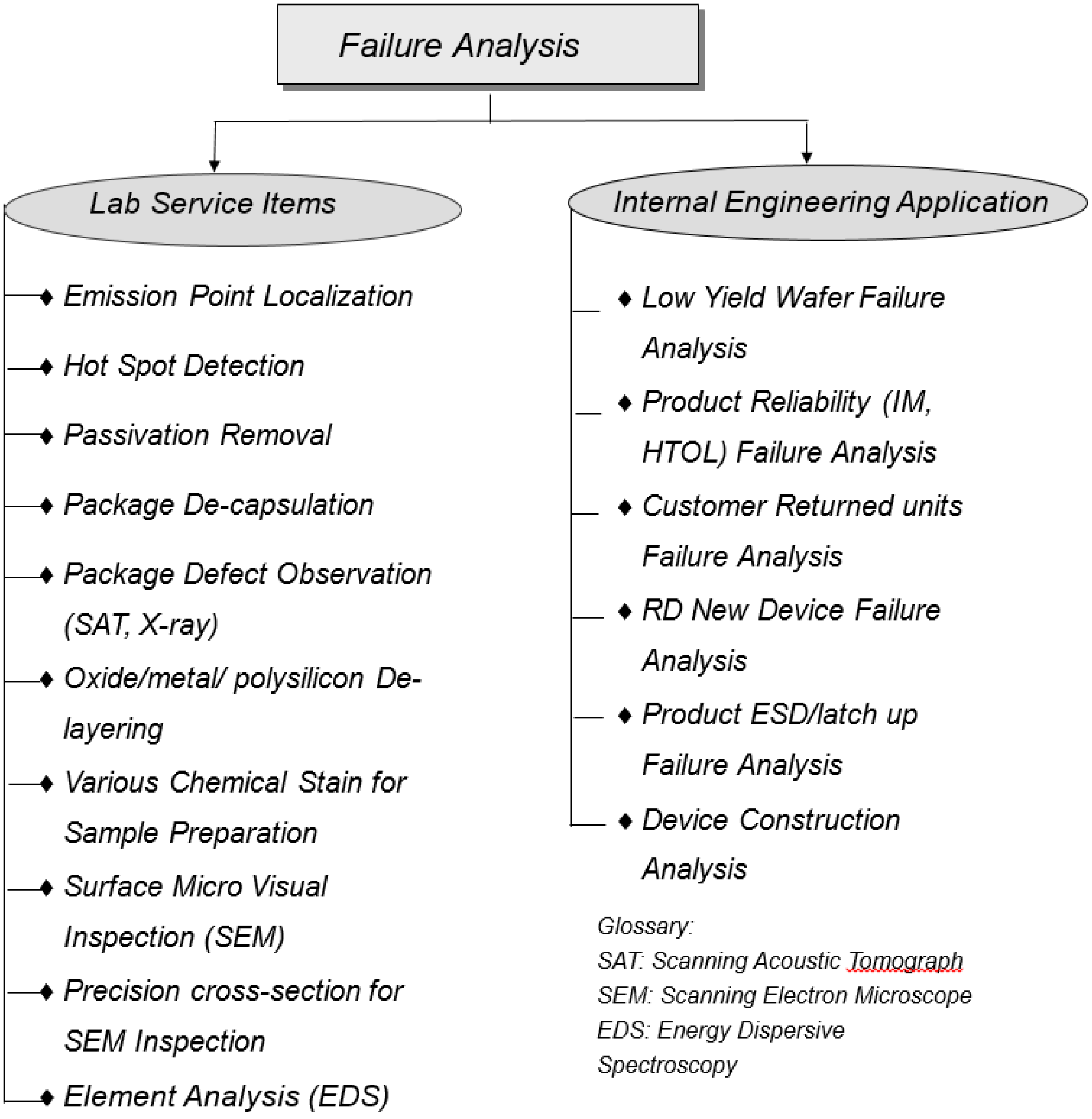
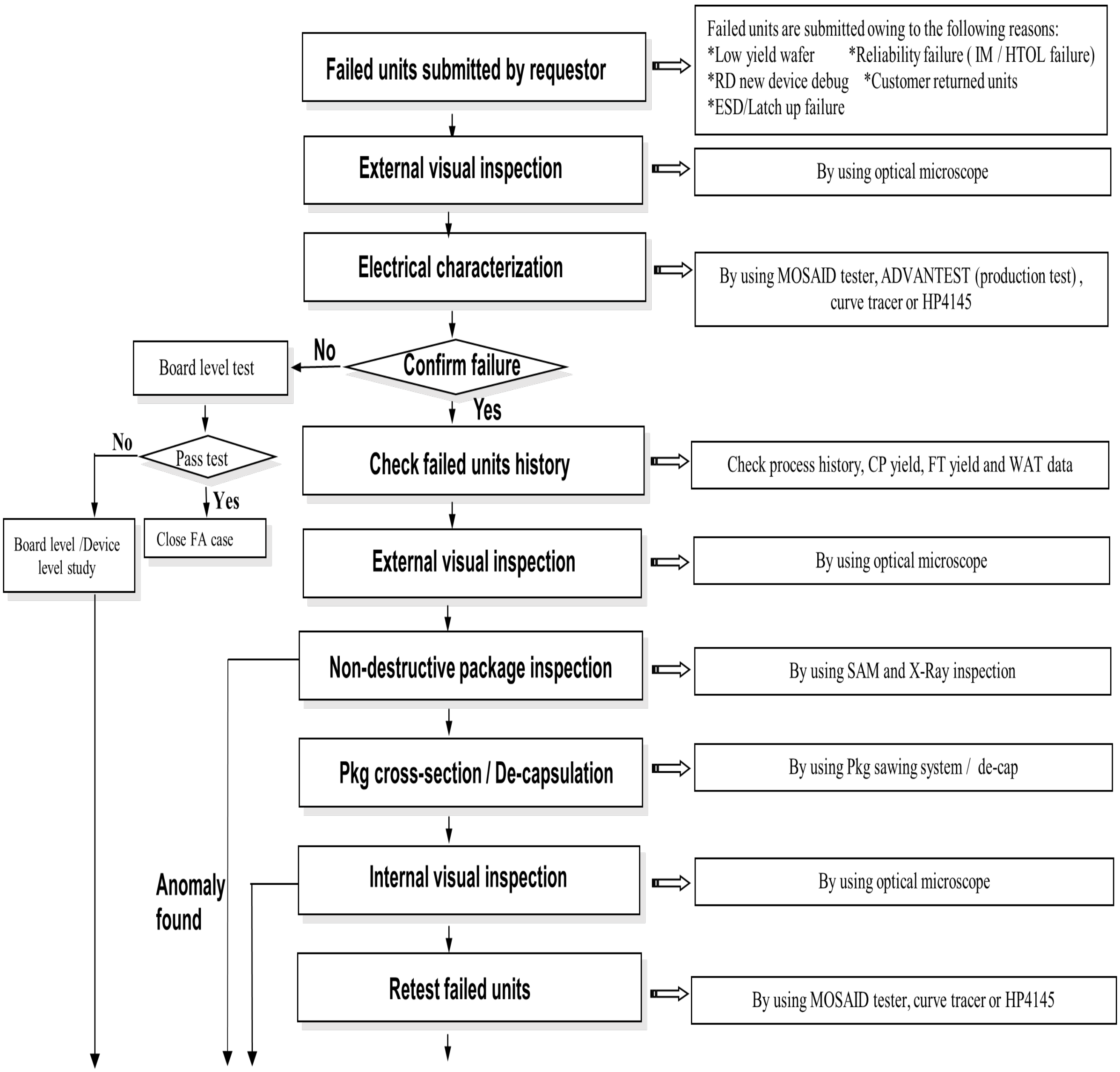


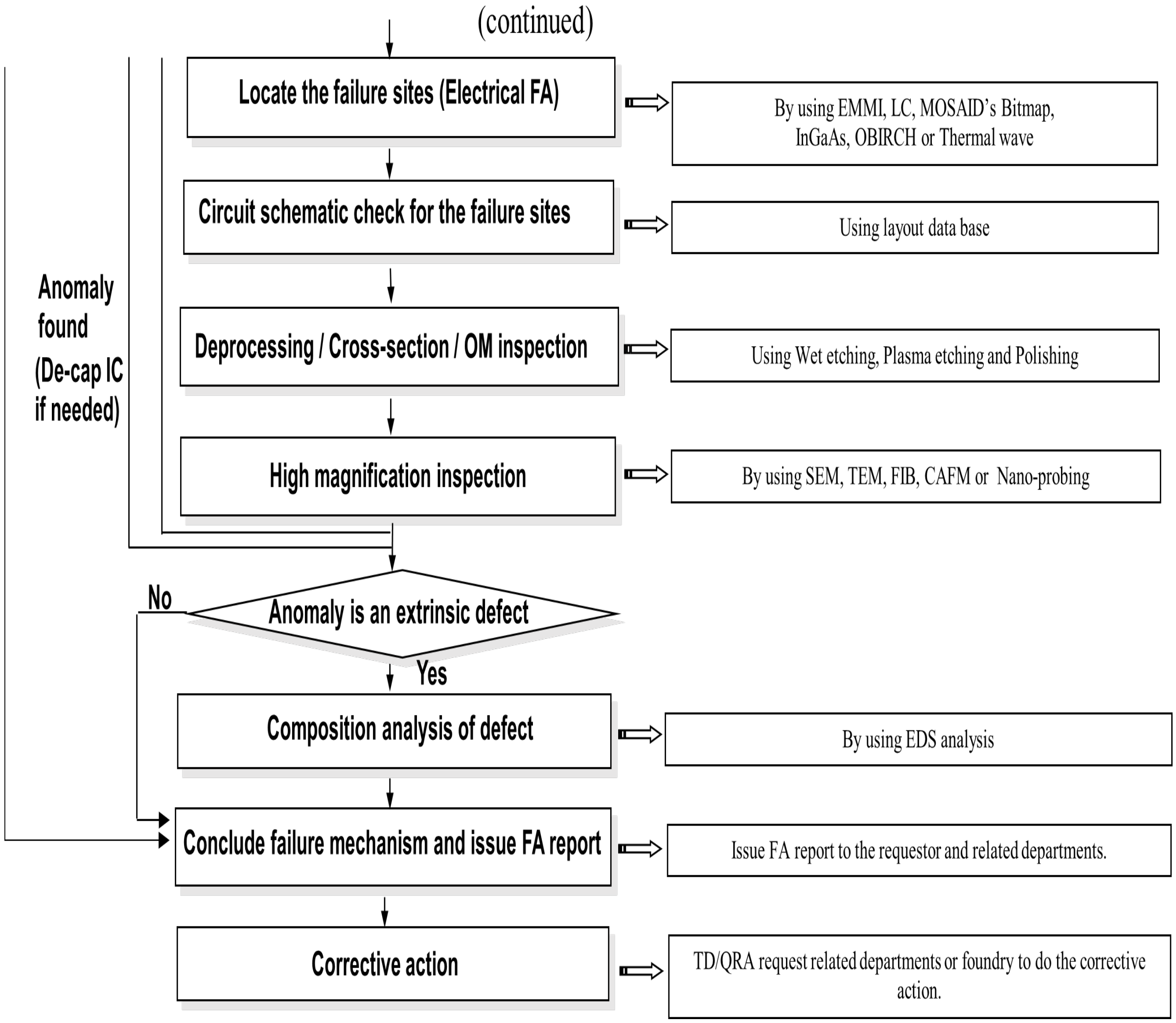
Figure 4-1 Failure Analysis Function

4.3 Failure Analysis Flow

A general failure analysis procedure is shown in Figure 4-2. The method demonstrated in the flow chart is utilized for all failure analyses.

ISSI Failure Analysis Flow





GLOSSARY:

SAM: Scanning Acoustic Microscope
EMMI: Emission Microscope with Si detector
LC: Liquid Crystal
InGaAs: Emission Microscope with InGaAs detector
OBIRCH: Optical Beam Induced Resistance Change
CAFM: Conductive Atomic Force Microscope
OM: Optical Microscope
SEM: Scanning Electron Microscope
TEM: Transmission Electron Microscope
FIB: Focus Ion Beam
EDS: Energy Dispersive Spectroscopy
FA: Failure Analysis

Figure 4-2 Failure Analysis Flow

4.4 Failure Analysis Instruments

As ULSI integration is becoming more complicated, analytical techniques and instruments become more advanced and dedicated in dealing with process related problems. ISSI currently has owned all necessary analytical instruments as shown in Table 4-1 in assisting the solution search for process-related problems.

Table 1 FA Instrument List

Category	Instrument	Principle of operation	Applications
Electrical Failure Analysis Lab	**Emission Microscope (EMMI)**	Detection of visible light, near-IR light, which are emitted at the defect sites.	Light spot localization for device leakage.
	Emission Microscope with InGaAs detector	Detecting longer wavelength of near-IR light, which is emitted at the defect sites.	Light spot localization for device leakage.
	Optical Beam Induced Resistance Change (OBIRCH)	Defect identification by detecting the change of resistance at defect site with scanning of a laser beam.	Localization of leakage current path Detection of vias/contacts' high resistance
	LC detection System	Use of nematic liquid crystals for failure analysis.	Hot spot localization for device leakage.
	Engineering MOSAID 4205	Tester contains precision instrumentation combined with advanced pattern and timing facilities.	Providing functional AC and DC parametric testing capabilities.
	Engineering ADVANTEST 5833		
	Parameter analyzer (Keithley 4200A) with Pulse Generator	Applying a variable voltage, current or waveform sources to a device and acquiring the I-V curve.	Device's I-V (current-voltage) characterization.
	Semi-Auto Probe Station	Motor-driven probe station in conjunction with temperature controller for wafer.	Pad probing. Thermal stressing.
	Manual Probe Station	Probe station with anti-vibration system for wafer.	
	Pico-Probe System	Use of micro-needle for internal circuit probing of chip.	Internal circuit probing of device.

	Wire bonding System	Using depressing force and ultrasonic vibration to make the Al wire bond for the metal pad of the chip.	Wire bonding for electrical analysis of device.
	Oscilloscope		Voltage waveform measurement.
Assembly Engineering Lab	**X-ray Radiography**	Image contrast based on the attenuation of an unfocused beam from a point source.	Inspection of the wire bonding, lead frame of packages.
	Scanning Acoustic Tomographs **(SAT)**	Observation of the internal interface by using ultrasonic waves.	Non-destructive analysis for package's interior.
Chemical Lab	**Reactive Ion Etching** **(RIE)**	Surface sputtering or etching of materials using accelerated ions of reactive gases.	To remove dielectric films such as Si_xN_y and Si_xO_y from devices.

Category	Instrument	Principle of operation	Applications
Physical Failure Analysis Lab	**Scanning Electron Microscope** **(SEM)**	Image from two dimensional intensity distributions of secondary electrons or back-scattering electrons from energetic e-beam.	Morphology observation. Micro structure analysis.
	Energy Dispersive Spectroscopy **(EDS)**	Attached to SEM equipment for detecting the radiation of characteristic X-ray.	Element detection. Composition analysis.
	Optical Microscope **(OM)**	Microscopy that magnifies images with a glass lens system.	For visual inspection of both wafer and package parts. A new microscope was moved in which can get wide depth of focus and do photo merge automatically.
	Laser Cutting System	Using laser beam with adjustable wavelength for material removal.	Quick and easy removal of various materials on device.
	Sputtering Coater	Thin film deposition by sputtering a gold/platinum foil.	SEM specimen coating for lowering surface charge effect.
	Polisher	Grinding with diamond paper.	Specimen preparation for cross-sectional and top-view observation.
Out-sourcing Instrument	**Transmission Electron Microscope** **(TEM)**	Microscopy that magnifies images using diffraction of transmitted electrons.	Structure analysis. Phase identification. Defect observation. Composition analysis.
	Focus Ion Beam **(FIB)**	Deposition or etching of the desired patterns onto the device surface using FIB.	Device circuit repairing. Precise cross-section specimen preparation.
	Optical Beam Induced Resistance Change (OBIRCH)	Defect identification by detecting the change of resistance at defect site with scanning of a laser beam.	Localization of leakage current path Detection of vias/contacts' high resistance
	Conductive Atomic Force Microscope (C-AFM)	Current sensing technique for electrical characterization of conductivity variations in resistive samples.	Detecting leakage or higher resistance of contact, junction etc.

	3-Dimensional computed Tomography X-ray (3D CT X-ray)	Image contrast based on the attenuation of an unfocused beam from a point source. A software program to build a volume by stacking the individual slices one on top of the other. The program may then display the volume in an alternative manner	Stereograph inspection of the wire bonding, lead frame, Sn ball or any interface of packages.
	Nano-probing system	Use of micro-needle for internal circuit probing of chip under SEM chamber and inspection.	Device internal circuit probing, measurement of transistor performance.
	Thermal Wave	Pinpointing failures by detecting heat emissions. The image detected by a high-sensitivity thermal emission detector (InSb detector).	Short-circuit of metal wires, Abnormality of contact holes, PKG short wires w/o de-capsulation, Oxide layer breakdown/leakage.

Emission Microscope with InGaAs detector

Emission microscope with InGaAs detector equipped with 5 lenses (0.8X ~100X) and having the capability of detecting visible light and near infrared light.

Figure 1

Field Emission Scanning Electron Microscope

Scanning electron microscope with electron gun of cold field emission and EDX system and having the resolution of 7 Å (at accelerated-voltage: 15KV).

Figure 2

Plasma Etcher (Reactive Ion Etching)

Reactive ion etching system with four process gases for isotropic or an-isotropic etching of silicon dioxide, silicon nitride and other materials using fluorine based gas.

Figure 3

Engineering Wire-Bonding System

Engineering Al wire-bonding system with auto-height detection and auto bonding function.

Figure 4

Dual Wavelength Laser Cutter

Laser cutter system with laser beams at two different wavelengths and with the function of single shot and continuous shots.

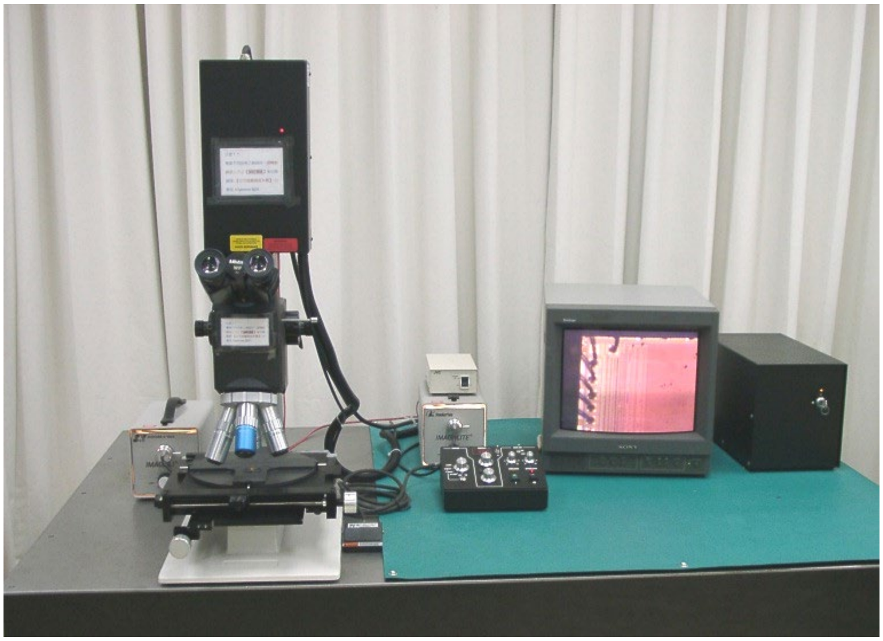


Figure 5

Polishing System

Polishing system with the function of bi-directional (clockwise and counterclockwise) rotation.

Reliability Assurance

In the highly competitive market of semiconductors, the requirement for IC component suppliers to deliver very reliable products has resulted in an overall philosophy of quality and reliability assurance. ISSI is committed to ship highly reliable products with reliability results well within specified and strict levels. To ensure the reliability standards, the rules of design, layout and processing are reviewed to cope with the new concepts during the early product development stage. Furthermore, new product/process qualifications and production reliability monitoring are performed in order to assure device performance and to accumulate statistical data.

Semiconductor Reliability

Below figure shows the time-dependent change in the semiconductor device failure rate. Discussions on failure rate change in time often classify the failure rate into three types of early, random and wear-out failure regions (the so-called “bathtub” curve). However, there is no clear definition for determining the boundary between these regions.

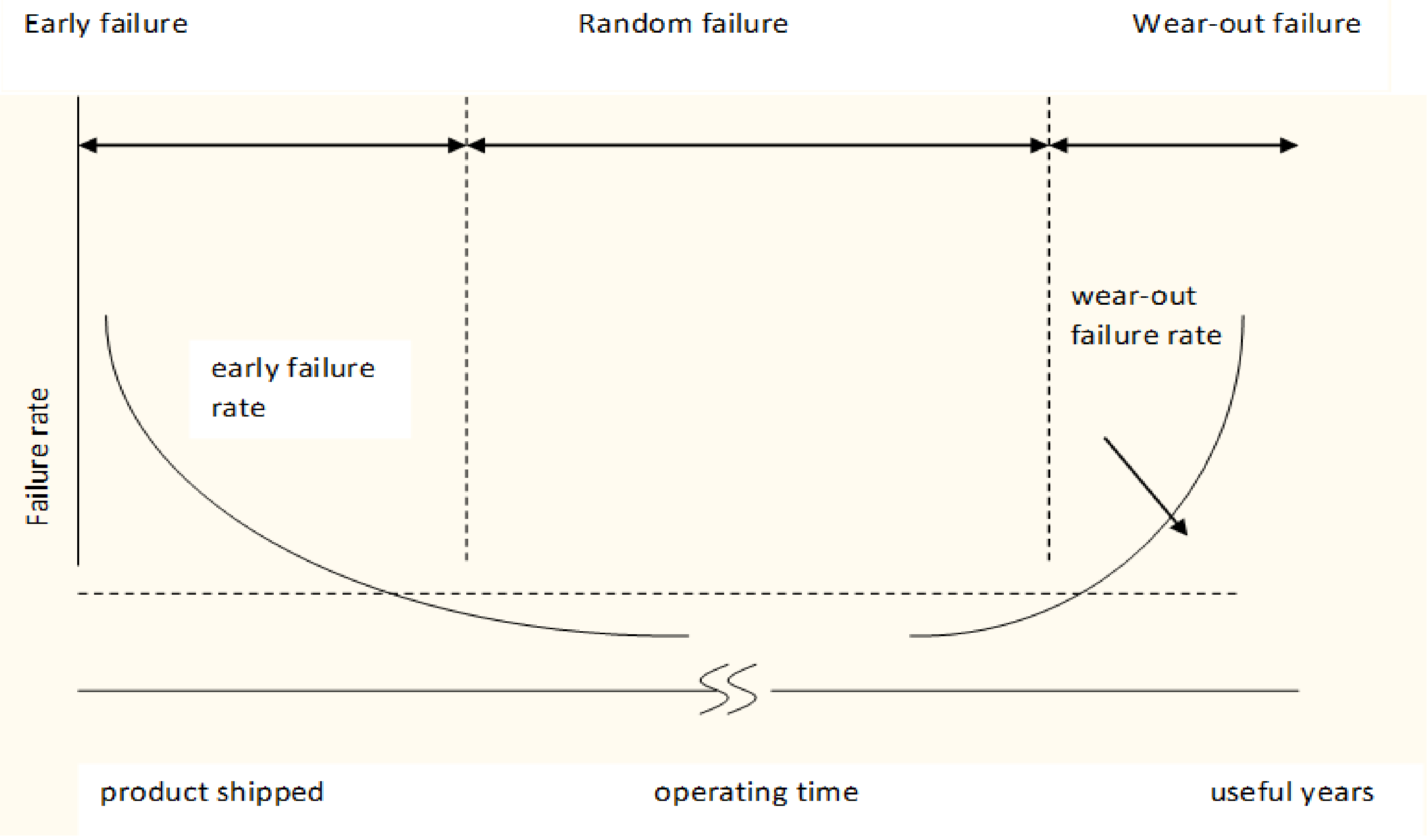


Figure 1: Time-Dependent Changes in Semiconductor Device Failure Rate

1.1 Early Failures

The failure rate in the early failure period is called the early failure rate (EFR), and exhibits a shape where the failure rate decreases over time. The vast majority of semiconductor device’s initial defects belong to those built into devices during wafer processing.

While most of these defects will be eliminated in the final sorting process, a certain percentage of devices with relatively insignificant defects may not have failed and may be shipped as passing products. These types of devices are inherently defective from the start and apt to fail when stress (voltage, temperature, etc) is applied for a relatively short period, and exhibit a high failure rate in a short time within the customer’s mounting process. However, these inherently defective devices fail and are eliminated over time, so the rate at which early failures occur decreases.

This property of semiconductor devices where the failure rate decreases over time can be used to perform screening known as “burn-in” where stress is applied for a short time in the stage before shipping to eliminate devices containing early defects. Products screened by burn-in not only improve the early failure rate in the market, but also make it possible to maintain high quality over a long period as long as these products do not enter the wear-out failure region.

1.2 Random Failures

When devices containing early defects have been eliminated to a certain degree, the early failure rate becomes extremely small, and the failure rate exhibits a constant level over time. In this state, the failure distribution is close to an exponential distribution, and this is called the random failure period.

The device failure rate is normally at a level that can be ignored for the most part. Most of the failures are due to devices containing relatively insignificant early defects (dust or crystal defects) that fail after a long time or random failures such as the memory soft error by alpha particles and other high-energy radioactive rays.

1.3 Wear-out Failures

Wear-out failures are failures rooted in the durability of the materials comprising semiconductor devices and the transistors, metal lines, oxide films and other elements. In this region, the failure rate increases with time until ultimately all the devices fail or suffer characteristic defects.

The main wear-out failure mechanisms for semiconductor devices are as follows:

Time-dependent dielectric breakdown (TDDB)

Hot carrier-induced characteristics fluctuation

Electromigration

Semiconductor device life is defined as the time at which the cumulative failure rate for the wear-out failure mode reaches the prescribed value, and is often determined by the reliability of each element comprising the device during the process development stage. These evaluation results are incorporated into design rules in the form of allowable stress limits to suppress wear-out failures in the product stage and ensure long-term reliability.

2 Failure Rate Calculation

Two functions are often used in the evaluation of reliability: probability density function (pdf) of failure $f(t)$ and failure rate $\lambda(t)$.

$f(t)$ denotes the probability of a device failing in the time interval dt at time t. It is related to the Cumulative Distribution Function (CDF), $F(t)$, as $f(t) = dF(t)/dt$.

On the other hand, failure rate $\lambda(t)$ is defined as the instantaneous failure rate of devices having survived to time t. Using the concept of conditional probability, P(B|A) = P(B and A both occur)/P(A), it can be derived that $\lambda(t)$ equals $f(t)/R(t)$ as shown below.

$$\text{instantaneous}\quad\text{failure}\quad\text{probability} = \frac{\text{fail in next }\Delta t}{\text{survive to }t} = \frac{F(t+\Delta t)-F(t)}{R(t)}$$

$$\text{instantaneous}\quad\text{failure}\quad\text{rate} = \lambda(t) = \frac{\lim\limits_{\Delta t\to 0}[\frac{F(t+\Delta t)-F(t)}{\Delta t}]}{R(t)} = \frac{f(t)}{R(t)}$$

In the following discussion, the failure rate calculation is described according to the stages of product lifespan.

2.1 Methods for Estimating the Early Failure Rate

Weibull distribution is applied to approximate the CDF of early failure period; it can exhibit a shape where the failure rate decreases over time.

Weibull distribution is characterized by two important parameters, scale factor (α) and shape factor (β). They are defined as:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] = 1 - R(t)$$

where t : life cycle or life time (EFR duration to failure)

α : scale factor or characteristic function

β : shape factor or shape parameter

Rearranging the equation, one obtains:

$$1 - F(t) = \exp\left[-\left(\frac{t}{\alpha} \right)^{\beta} \right]$$

$$\ln[1 - F(t)] = -\left(\frac{t}{\alpha} \right)^{\beta}$$

$$\ln[-\ln(1 - F(t)] = \beta \ln t - \beta \ln \alpha$$

When plotted in ln [- ln (1 – *F(t)*)] against *t* on log scale (Below figure) , the data should approximately fall on a straight regression line. Scale factor α can be obtained from the intercept of the straight line; it is constant for a fixed test condition. Shape factor β is the slope of the straight line and its value is less than one for early failure period.

Using the relationships that $f(t) = dF(t)/dt$ and $\lambda(t) = f(t)/R(t)$, one can derive the failure rate as:

$$\lambda(t) = \frac{\beta t^{\beta - 1}}{\alpha^{\beta}}$$

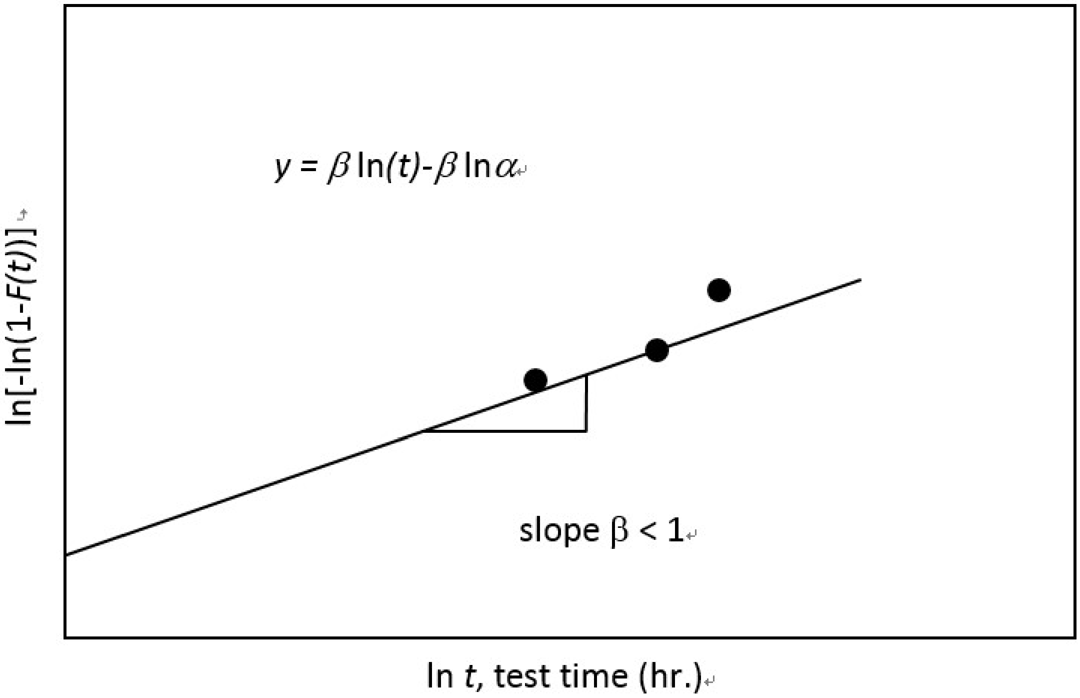


Figure 2 - ln t, test time (hr.) VS ln[-ln(1-F(t))]

2.2 Methods for Estimating the Useful Life Failure Rate

When devices containing early defects have been eliminated to a certain degree, the initial failure rate becomes extremely small, and the failure rate exhibits a gradually declining curve over time. The failure rate at this period is obtained by dividing the number of failures observed by the device hours, usually expressed as failures per billion device hours (FITs). This is called point estimate because it is obtained from observation on a portion (sample) of the population of devices. In order to determine the unknown population parameter from known sample statistics, it is necessary to make use of specific probability distribution. The chi-square distribution (χ^2) that relates observed and expected frequencies of an event is frequently used. The relationship between failure rate at stress conditions and the chi-square distribution is shown in the following formula:

$$\lambda_{stress} = \frac{\chi^2(\alpha, n)}{2t}$$

where:

λ_{stress} = failure rate at stress conditions

χ^2 = chi-square function

α = (100 - confidence level) /100

n = degree of freedom = $2r + 2$

r = number of failures

t = device hours

The chi-square values for α equal to 60% and 90% at r between 0 and 12 are shown in below table.

Chi-Square Distribution Function			
60% Confidence Level		**90% Confidence Level**	
No. Fails	χ^2 Quantity	No. Fails	χ^2 Quantity
0	1.833	0	4.605
1	4.045	1	7.779
2	6.211	2	10.645
3	8.351	3	13.362
4	10.473	4	15.987
5	12.584	5	18.549
6	14.685	6	21.064
7	16.780	7	23.542
8	18.868	8	25.989

Since all the reliability tests are performed under accelerated stress condition, it is important to evaluate the acceleration factor of different stresses.

1) Thermal Acceleration Factor

Acceleration factor for thermal stress is calculated using the Arrhenius equation:

$$AF_t = e^{[\frac{E_a}{k}(\frac{1}{273+T_{use}} - \frac{1}{273+T_{stress}})]}$$

where: AF_t = thermal acceleration factor

E_a = activation energy in electron Volts (eV)[2],

k = Boltzmann's constant 8.62 x 10^{-5} eV / °K

T_{use} = junction temperature at normal use condition in °C

T_{stress} = the stress temperature in °C

2) Voltage Acceleration Factor

High electrical field can cause physical damage in the oxide layers. The acceleration factor due to voltage stress is a function of both the stress voltage, V_{stress}, and the wafer process. AF_v can be derived from Eyring model as:

$$AF_v = e^{\gamma(V_{stress} - V_{use})}$$

where: AF_v = voltage acceleration factor

γ = constant in 1/V

V_{stress} = stress voltage

V_{use} = use voltage

---

[2] The activation energy is defined as the excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur. Examples are the energy needed by the molecule to take part in a chemical reaction, by an electron to reach the conduction band in a semiconductor, or by a lattice defect to move to a neighboring site. (Ref. *Van Nostrand's Scientific Encyclopedia*) ISSI's failure rate calculations are based on acceleration from high temperature where thermal activation energy, Ea, is typically identified in JEDEC Standard.

3 Humidity Acceleration Factor

For humidity acceleration test, the acceleration factor can be estimated by

$$AF_h = \left(\frac{RH_{stress}}{RH_{use}} \right)^m$$

where : RH_{stress} = relative humidity in stress

RH_{use} = relative humidity in use (typical value 17.6%)

m = experimentally determined (typical value $m = 3$)

If temperature is included in the humidity test, both temperature and humidity acceleration factor need to be considered.

In THB test (Temp/Humidity/Bias), the voltage acceleration factor must be added. The junction heating effect can reduce the relative humidity. For example, a 5°C junction heating effect by bias can reduce the RH from 85% to 73%.

4 Temp Cycling Acceleration Factor

The acceleration factor can be estimated by

$$AF_{tc} = \left(\frac{T_{\max,stress} - T_{\min,stress}}{T_{\max,use} - T_{\min,use}} \right)^n$$

where : $T_{max,\ stress}$ = high temp in cycling stress

$T_{min,\ stress}$ = low temp in cycling stress

$T_{max,\ use}$ = high temp in field application, usually 70°C

$T_{min,\ use}$ = low temp in field application, usually 0°C

n = experimentally determined, usually $n = 5$

5 MTTF at Use Conditions

The mean-time-to-failure (MTTF) is defined as the average time-to-failure (or expected time-to-failure) for a population of devices, when operating its required function under the specified conditions for a stated period of time. It can be expressed by:

$$\mathrm{MTTF} = \int_0^\infty t f(t)\,dt$$

The overall relationship of *F*(*t*), *R*(*t*), *f*(*t*), λ(*t*) and MTTF can be depicted as below figure.

R(*t*) + *F*(*t*)

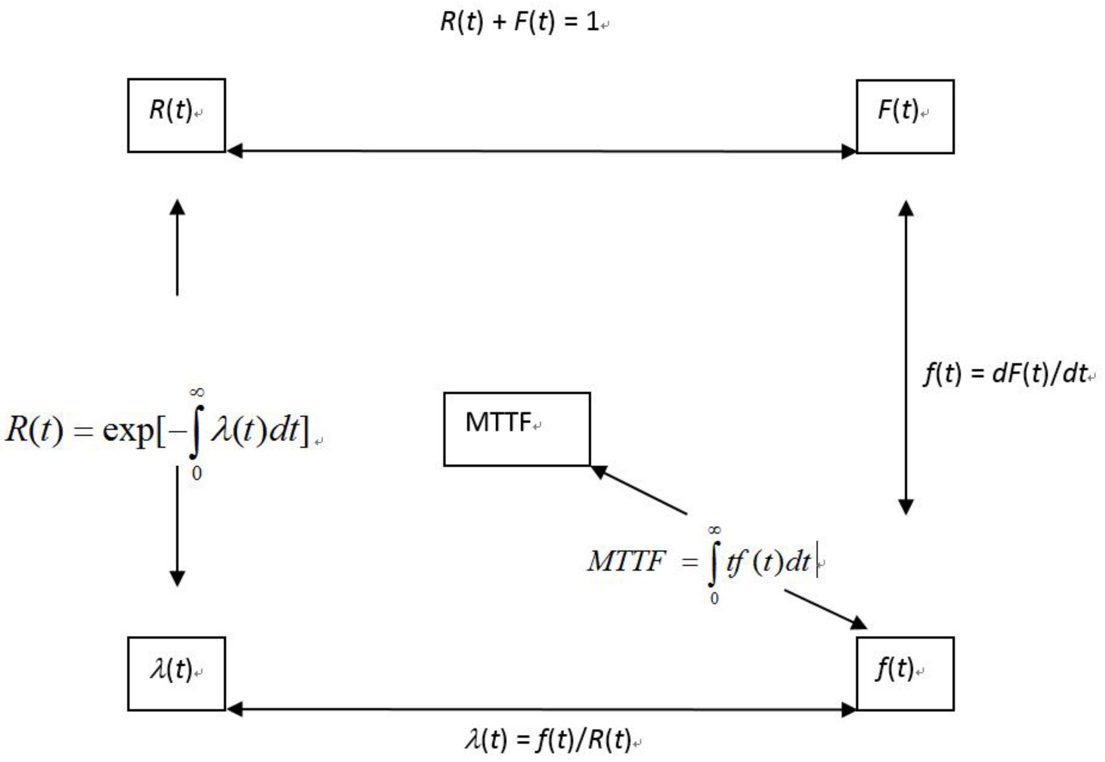


Figure 3 - The overall relationship of F(t), R(t), f(t), ⍰(t) and MTTF

For the case of constant failure rate ($\lambda(t)$ = constant), $R(t) = \exp(-\lambda t)$, $F(t) = 1 - \exp(-\lambda t)$ and $f(t) = dF(t)/dt = \lambda \exp(-\lambda t)$

$$\mathrm{MTTF} = \int_0^\infty t f(t)dt = \int_0^\infty t\lambda \exp(-\lambda t)dt = \frac{1}{\lambda_{use}}$$

where the point estimate of the failure rate at use conditions is calculated as:

$$\lambda_{use} = \frac{\lambda_{stress}}{AF_t \times AF_v}$$

New Product/Process Qualification

The products used for reliability testing are representative of all device families, package families, foundry locations, and assembly locations. The standards referenced by ISSI are JEDEC Standard 22 and MIL-STD-883, which have been universally used throughout the semiconductor industry.

Reliability is defined as the probability that a semiconductor device will perform its required function under the specified conditions for a stated period of time. The probability of survival prior to time t, R(t), plus the probability of failure, F(t), is always unity. Expressed as a formula:

R(t) + F(t) = 1, or R(t) = 1- F(t)

The probability of survival and failure is derived from the observed results of actual stress tests performed on the devices. High Temperature Operating Life (HTOL) will determine the expected failure rate, λ(t), under operating conditions. The other reliability tests, which are described in below, accelerate other expected conditions and contribute further survival /failure rates for both die/process and package.

1.1 Die/Process Reliability Tests

1) High Temperature Operating Life Test (HTOL)

(Refer to JEDEC 22-A108)

High temperature operating life test is performed to accelerate failure mechanisms that are activated by temperature while under bias. This test is used to predict long-term failure rates since acceleration by temperature is understood and the calculation for acceleration factor is well established. Prior to HTOL, all test samples are screened to standard electrical tests at low temperature and high temperature with prior burn-in. Dynamic operating conditions are applied to most cases and the test circuit is depending on the specific device. The typical stress voltage is 1.1 times of normal operating voltage. Unless otherwise specified, the stress temperature is maintained at 125 ℃. Devices are tested at prescribed time-points. Failure rates are calculated in terms of FITs (failures in time). Each FIT represents one failure in 109 device-hours.

2) Infant Mortality (IM)

Infant mortality testing determines the early failure rate of a specific product and process. The test conditions are basically the same as the high temperature operating life test with an increased sample size to ensure an accurate failure rate. The test temperatures **Tj** can be set between 125 ℃to 150 ℃, depending on product type and the test environment. The typical stress voltage is at least 1.2 times of normal operating voltage. The failure rate data is used to determine a product burn-in strategy for each product and provide information for process improvement.

3) Electrostatic Discharge (ESD)

(Refer to ANSI/ESDA/JEDEC JS-001 and JS-002)

Electrostatic discharge sensitivity (ESD) tests are designed to measure the sensitivity of each device with respect to electrostatic discharges that may occur during device handling. Various test methods have been devised to analyze ESD. Currently, ISSI evaluate ESD using the following test methods. The human body model (HBM) is in accordance with the standard specified by ANSI/ESDA/JEDEC JS-001 while the charge device model (CDM) is by ANSI/ESDA/JEDEC JS-002.

The human body model is based on a high-voltage pulse (positive and negative) of longer duration, simulating discharge through human contact. The charge device model is based on the phenomenon where the semiconductor device itself carries a charge or where the charge induced to the device from charged object near the device is discharged. It reproduces the discharge mechanism in the form closest to the discharge phenomenon occurring in the field.

4) Latch-up

(Refer to JEDEC standard No. 78)

The latch-up test is designed specifically for CMOS processed devices to detect parasitic bipolar circuits that, when activated, may short power and ground nodes. Test conditions are significantly worse than normal operation variations to provide a margin for safe operation. Presently, ISSI evaluates latch-up based on JEDEC standard No. 78. For JEDEC standard, current (positive and negative) is injected into individual input/output pins in steps while the power supply current is monitored. The current into the test pin must rise to a minimum of 100 mA without a latch-up condition.

5) Soft Error Rate

(Refer to JEDEC Standard 89)

Semiconductor memory defects that can be recovered by rewriting the data are called soft errors. In addition to being caused by the power supply line and ground line noise, soft error are also caused by α-rays emitted from the trace amounts of uranium, thorium and other radioactive substances contained in the package or wiring materials.

There are two methods for evaluating soft errors: system tests which consist of actually operating large number of samples, and accelerated tests using a α-ray source.

When evaluating the absolute soft error value it is necessary to conduct system tests. However, system tests require many samples and long times (typically, 1000 samples and 1000 hours or more).

In contrast, accelerated tests allow evaluation in a short time, but have the problem that it is difficult to accurately obtain accelerated characteristics for a market environment.

Soft error rates are expressed in FIT units:

1 FIT = 1 Failure/109 Device-hours

6) Endurance Cycling

(Refer to MIL-STD-883 1033, JEDEC 22- A117)

The test is used to evaluate the quality of the tunnel oxide of Flash products. Continued program-erase operation can cause charge trapping or even breakdown in the tunnel oxide, resulting in threshold shift and eventually failure of a cell to retain data. The test requires typical 100k cycles at room temperature and high temperature. Large electrical field changes between the gate and drain of the memory cell can also cause damage of the oxide layer.

7) Data retention

(Refer to JEDEC 22- A117, JESD 47)

The test is to measure the stability of electron in the floating gate of Flash products. Devices are exposed to high temperature, typically, 125 or 150 ℃, which causes acceleration of charge loss or gain, resulting in shifting of threshold voltage. No bias is needed for this test. Charge trapping or defect in tunnel oxide and other dielectric, mobile ion contamination may contribute to the degrading of data retention performance.

8) High Temperature Storage Life Test (HTSL)

(Refer to JEDEC 22-A103)

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Unless otherwise specified, the stress temperature is maintained at 150 °C.

1.2 Package Reliability Tests

1) Highly Accelerated Stress Test (HAST)

(Refer to JEDEC 22 - A110)

The highly accelerated stress test provides constant multiple stress conditions including temperature, humidity, pressure, and voltage bias. It is performed for the purpose of evaluating the reliability of non-hermetic packaged devices operating in the humid environments. The multiple stress conditions accelerate the penetration of moisture through the package mold compound or along the interface between the external protective materials and the metallic conductors passing through package. When moisture reaches the die surface, the applied potential establishes an electrolytic condition that corrodes aluminum conductors and affects DC parameters of the device. Presence of contaminants on the die surface such as chlorine greatly accelerates the corrosion process. Additionally, excessive phosphorus in the passivation will react under these conditions.

2) Unbiased Autoclave (Pressure Cooker Test)

(Refer to JEDEC 22- A102)

The autoclave test is performed to evaluate the moisture resistance of non-hermetic packaged units. Devices are subject to pressure, humidity, and elevated temperature to accelerate the penetration of moisture through the molding compound or along the interface of the device pins and molding compound. Expected failure mechanisms include mobile ionic contamination, leakage along the die surface, or metal corrosion caused by reactive agents present on the die surface. The autoclave test is performed in a pressure chamber capable of maintaining temperature and pressure. Steam is introduced into the chamber until saturation, then the chamber is sealed and the temperature is elevated to 121 °C, corresponding to a pressure of 30 psia (2 atm). This condition is maintained for the duration of the test. Upon completion of the specified time, the devices are cooled, dried and electrically tested. (Note: PCT is not applied for organic substrate package.)

3) Temperature Cycling Test (TCT)

(Refer to JEDEC 22- A104)

Temperature cycling test accelerates the effects that changes in the temperature will cause damage between different components within the specific die and packaging system due to different thermal expansion coefficients. Typical examples of damage caused by this test include package cracking, cracking or cratering of the die, passivation or metal de-lamination, and more subtle damage resulting impaired electrical performance. During testing devices are inserted into a chamber where the interior is cycled between specified temperatures and held at each temperature for a minimum of one minute. Temperature extremes depend on the condition selected in the test method. The total stress corresponds to the number of cycles completed at the specified temperature.

4) High Temperature Storage Life Test (HTSL)

(Refer to JEDEC 22-A103)

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Unless otherwise specified, the stress temperature is maintained at 150 ℃.

5) Preconditioning Test (Moisture Sensitivity)

(Refer to JEDEC 22- A113 , J-STD-020)

Surface mount packages may be damaged during the solder reflow process when moisture in the package expands rapidly. Two test methods are utilized to determine which packages may be sensitive and what level of sensitivity exists. JEDEC test method A113 establishes the reliability of devices exposed to a specified preconditioning process at various moisture levels by subjecting preconditioned devices to HAST, PCT and TCT. The test result determines whether dry packing is necessary to ensure the reliability of the product after the assembly process.

6) Solderability

(Refer to J-STD-002)

The solderability test is used to determine the ability of package leads wetted by solder. This test verifies that the method of lead treatment to facilitate solderability is satisfactory and will allow successful solder connection to designated surface. (A) For Lead Frame package, the test is accomplished by immersing leads in flux then dipping the leads into molten solder of 215℃ ± 5℃ for non Pb free or 245℃±5 ℃for Pb free. No less than 95% coverage of the dipped area should be shown on each lead. (B) For Substrate package, the reflow temperature IR Reflow Soldering is Pb-free: 230~245℃ and SnPb: 215~230℃.

7) Mark Permanency

(Refer to JEDEC 22-B107)

The mark permanency test subject’s package marking to solvents and cleaning solution commonly used for removing solder flux on circuit boards to ensure the marking will not become illegible. Devices and a brush are immersed into one of three specified solvents for one minute, and then removed. The devices are then brushed ten strokes. This process is repeated three times for each group of solvents and devices. After they are rinsed and dried, the devices are examined for legibility according to specified criteria.

8) Lead Integrity

(Refer to JEDEC 22-B105)

The lead integrity test provides tests for determining the integrity of devices leads, welds and seals. Devices are subject to various stresses including tension, bending fatigue and torque appropriate to the type of lead. Devices are then examined under optical microscope to determine any evidence of breakage, loosening or motion between the terminal and device body.

9) Solder Ball Shear

(Refer to JEDEC 22-B117)

This test method is used to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment, and end-use conditions.

10) Bond Pull and Shear

(Refer to MIL-STD-883, Method 2011)

The purpose of these tests is to measure bond strength, evaluate bond strength/bond strength distributions or determine compliance with specified bond strength requirements of the applicable acquisition document.

Qualification Test Method and Acceptance Criteria

The summary shown in following tables give brief descriptions of the various reliability tests. Not all of the tests listed are performed on each product and other tests can be performed when appropriate.

Table 1: Qualification Test Method and Acceptance Criteria

	Test item	Applied with	Test method	Test condition	Sample #(Min) x lot	Acc No	Comments
1	HTOL High Temp. Operating Life	All ISSI products.	JEDEC 22 A108 MIL-STD-883 1005	T=125℃, Apply Voltage ≧Vcc max, Dynamic	77x3	0	Acceptable number is upon sample size. For Memory: Target failure rate < 100 FITs at 60% CL after 1 Khrs.
2	ESD Electrostatic Discharge	All ISSI products.	ANSI/ESDA/JEDEC JS-001 ANSI/ESDA/JEDEC JS-002	Human Body Model (HBM) R=1.5kohm, C=100pF. Charge Device Model (CDM).	3x1 HBM 3x1 CDM	0 0	3 samples for each test mode HBM ≧ ±2000V. CDM≧±500V (corner pins >= ±750V) for SRAM/DRAM Automotive devices 3pcs for each voltage level for Analog

3	LU Latch-up	All ISSI products.	JEDEC STD No. 78	Current trigger Voltage trigger	3x1 3x1	0 0	(I trigger) ≧ ± 100 mA (V trigger) ≧ + 1.5x Vcc or MSV, which is less.
4	IM Infant Mortality	DRAM / SRAM		T=125℃, Vcc applied upon device types, Dynamic.	1300x1	Optional	Target failure rate < 100 FITs after 96 hrs at 60% CL.
5	SER Soft Error Rate	≧1M DRAM / SRAM	MIL-STD-883 1032 JEDEC 89	Source: Alpha particle Am-241, test patterns: checker board or reverse checkerboard at room temp.	3x1	< 1K MFITs **	**Remark: 1. The SRAM with ECC function < 10 FITs/Mbit. 2. Other devices target failure rate < 1000 FITs/Mbit at 60% CL.
6	HTSL High Temp. Storage	All ISSI products	JEDEC 22 A103 MIL-STD-883 1008 JEDEC22-A117	T=150℃, 1000hrs	25x3**	0	** S/S=77ea for Flash/pFusion.
7	HAST Highly Accelerated Stress Test	All ISSI products .	JEDEC 22 A110	T=130℃, 85%RH, 33.3 psia, Apply Voltage≧VCC max, 96hrs min.(or T=110℃, 85%RH, 17.7psia , Apply Voltage≧VCC max, 264 hrs)	25x3	0	Use LTPD 10% For Analog: S/S=77ea Use LTPD=5%, no failure is allowed.
8	PCT Pressure Cooker (or Autoclave)	Non BGA pkg types	JEDEC 22 A102	T=121℃, 100%RH, 30psia 168 hrs	25x3	0	Use LTPD 10% For Analog: S/S=77ea Use LTPD=5%, no failure is allowed.
9	TC Temperature Cycling	All pkg types	JEDEC 22 A104 MIL-STD-883 1010	T=-65℃ to 150℃, 250 cycles (Or equivalent -55C to 125℃, 700-1000 cycles)	25x3	0	Use LTPD 10% For Analog: S/S=77ea Use LTPD=5%, no failure is allowed.

10	PC Pre-conditioning	All pkg types	JEDEC 22 A113	Bake 24hrs @+125℃, moisture soak (level 3: 192 hrs@30℃ /60%RH), reflow solder IR @ (a) For non Pb-free: 240+5/-0℃, (b) For Pb-free: 260 +5/-0℃,	77 x3	1	Use LTPD 5%. The parts, passed level 3 test, will be used to do HAST, T/C, PCT. Level 1 & 2 are optional. S/S=231ea for Analog.
11	PD Physical Dimensions	All pkg types	JEDEC 22 B100 MIL-STD-883 2016		10x3	0	Cpk≧1.67
12	SD Solderability	only for L/F package	J-STD-002	1. Steam aging - Temp : 93+3/-3°C, Time : 8±0.25 hrs. (Optional) 2. For non Pb-free T=215±5℃, and For Pb-free T=245±5℃, Dwell time = 5±0.5sec,	15x1	0	Lead coverage area > 95%
13	IR Reflow Soldering	only for substrate package	J-STD-002	1. Steam aging - Temp : 93+3/-3°C, Time : 8±0.25 hrs. (Optional) 2. Reflow Temp: a.Pb-free: 230~250°C b.SnPb: 215~230°C	15x1	0	Use LTPD=15%. No failure is allowed.
14	LI Lead Integrity	For through-hole devices only	JEDEC 22-B105 MIL-STD-883 2004	1) 2 oz for SOJ and TSOP, 8 oz for other Pkg 2) for bending arc = 90 ±5 degree 3) 2 cycles for TSOP, 3 cycles for other Pkg	5x1**	0	No failure **45 leads of 5
15	Mark Permanency	All pkg w/ ink marking**	JEDEC 22 B107 MIL-STD-883 2015		5x1	0	Use LTPD 50% ** Except BGA with Laser Marking.
16	WBP Wire Bond Pull	Option to all pkgs	MIL-STD-883 Method 2011		5x1**	0	Ppk≧1.66 or Cpk≧1.33 Strength≧ 3gram For all product, Bond pull SPEC has depend on wire diameter, **30 bonds from a minimum of 5 devices
17	WBS Wire Bond	Option to all pkgs	AEC Q100-001		5x1**	0	Bond shear strength not less than 30 gram.

	Shear		MIL-STD-883 2011				**30 bonds from a minimum of 5 devices
18	CO Co-planarity	Only for SMD pkg	JEDEC 22 B108	1) Measured accuracies within ± 10% of specified deviation	5x1	0	Failure specification. Deviation=4 mil.
19	SBS Solder Ball Shear	Substrate type package	AEC Q100-010 JEDEC 47		10x3**	0	Ppk>=1.66 or Cpk>=1.33 **5 balls from a min. of 10 devices

Table 2 : Qualification Test Method and Acceptance Criteria (Nonvolatile)

	Qualification Test	**Test Method**	**Test Conditions**	**Samp. Size**	**Rej. No.**	**Lots Req.**	**Comments**
1	NVCE Endurance Cycle	JEDEC22-A117	1) T=85℃/25℃ 2) V=Vcc Max 3) Cycling 100K for Flash and 10K for pFusion.[*1] (MTP: 20K)[*1]	39/38	0[*2]	3	For Flash and eFusion. (Not apply to OTP).
2	HTDR(Data retention after Cycling)	JESD47 JEDEC22-A117	1) T=125℃ 2) 10/100hrs	39	0[*2]	3	For Flash and pFusion only (Not apply to OTP)
3	LTDR (Read stress after cycling)	JESD47 JEDEC22-A117	1) T=Room temp 2) 500hrs	38	0[*2]	3	For Flash and pFusion only (Not apply to OTP)

[*1] Specific cycling SPEC refers to product datasheet.

[*2] A/R: the reject criteria maybe different from case to case per the discussion with foundry for eFusion.

Table3 : Test upon request or optional test

	Qualification Test	Applied to	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments
1	Resistance to Solder Heat	option to all pkgs	JEDEC 22 B106 MIL-STD-750 2031	T=260±5℃ t=10+2/-0 sec. lead immersion is 0.05”.	5	0	1	Package related test.
2	Salt Atmosphere	option to all pkgs	MIL-STD-883 1009	T=35℃, 5% NaCl t=24hrs	5	0	1	Package related test.
3	Pressurizing body	option to all pkgs	EIAJ ED4702	Load: 10N Time: 10±1sec Pressurizing jig : R0.3cm	22	0	1	Criteria: F/T test
4	Vibration	option to all pkgs	JESD22-B103	Frequency : 20 ~ 2000Hz Acceleration : 20G peak Displacement : 1.52mm Sweep time : 20 ~ 2000 ~ 20Hz in 4 mins Duration : 4 times per X,Y,Z axis, Total : 48 mins	11	0	1	Criteria: F/T test

Table 4 : Level 2 / Board level test (Selective)

	Qualification Test	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments	Note
1	Bending	IPC-JEDEC-9702	1) Daisy-Chain package 2) Travel speed: 1~1.42mm/sec which depends on board thickness 3) Strain rate : >5,000µstrain/sec 4) Give weibull slope	22	0	1	20% change in resistance	By request
2	Shock (Drop Test)	JESD22-B111	1) Daisy-Chain package 2) Use event detector 3) 3 shock for each top and bottom face 4) 340 G For hand product: 5) 30 shock for 4 face 6) 1500G, half-sine	15 per board	0	1	10% change in resistance	By request
3	Solder Joint Life Test	IPC-JEDEC-9701	1) Daisy-Chain package 2) T= -0 to 100℃ Hand product: T= -40 to 125℃ 3) Temp slope= 10 ℃/ min, Dwell T= 10 min 4) Real-Time Measurement	32 virgin + 10 rework	0	1	20% change in resistance Pass 3500 cycles 32 (Virgin sample) and 10 (Rework sample)	By request
4	Solder Joint Strength	IPC-JEDEC-9701	1) T=-0 to 100℃. 2) Temp slope= 10℃/ min, Dwell T= 10 min 3) Pull test	5	0	1	Pass 3500 cycles Bond pull strength not less than 3 gram	By request

The qualification for automotive application should follow the requirements of AEC-Q100. The test items of reliability qualification for automotive are shown as following:

Table 5: Automotive Qualification Test Method and Acceptance Criteria

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
HTOL (High Temp. Operating Life)	AEC-Q100#B1	JESD22A108	77 X 3 lots	0 fail	Grade 1 : T=125°C, 1000 hrs. Operation mode with Vcc max stress at least. F/T check before and after at low, and high temp. Should do Cycling test before HTOL for Flash/pFusion.
ELFR (Early Life Failure Rate)	AEC-Q100-008	JESD22A108	800 X 3 lots	0 fail	Grade 1 : T=125℃, 48 hrs. Operation mode with Vcc max stress at least. F/T check before and after at low, and high temp.
HTSL (High Temp. Storage Life)	AEC-Q100#A6	JESD22A103	45 X 3 lot **	0 fail	Grade 2 : 150℃, 1000 hrs. F/T check before and after at high temp. **Should do cycling test before HTSL with S/S=77ea and 3 lots if it's for cover HTDR for Flash/pFusion.
SER (Soft Error Rate)	AEC-Q100#E11	JESD89-1,-2,-3	3 X 1 lot	< 1k FITs/Mbit	For devices with memory sizes >= 1 Mbits SRAM or DRAM based cells. ** The SRAM with ECC function < 10 FITs/Mbit.
Endurance Cycle	AEC-Q100-005	JEDEC22-A117	77 x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=85℃/25℃ 2) V=Vcc Max 3) Cycling 100K for Flash and 10K for pFusion.* (MTP: 20K)

HTDR (High Temperature Data Retention)	AEC-Q100-005	JEDEC22-A117	77 x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=125℃ 2) 10/100hrs. Remark: HTDR can be covered by cycling+HTSL.
LTDR (Low Temperature Data Retention Storage Life)	AEC-Q100-005	JEDEC22-A117	77x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=Room temp storage 2) 1000hrs

*Remark: Some specific devices with different cycling count SPEC should follow the statement in the datasheet.

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
ESD HBM	AEC-Q100-002	ANSI/ESDA/JEDEC JS-001	3 devices for each step X 1 lot	±2 kV	F/T check before and after at high temp (IV curve check for every 500V)
ESD CDM	AEC-Q100-011	ANSI/ESDA/JEDEC JS-002	3 devices for each step X 1 lot	±500 V (corner pins ≧ ±750V)	F/T check before and after at high temp (IV curve check)
Latch-up	AEC-Q100-004	JESD78	6 devices X 1 lot	±100mA +1.5 X max Vcc or MSV, which is less	F/T check before and after at high temp (Icc variation between initial and after trigger)

Table 6: Automotive Qualification Test Method and Acceptance Criteria (package portion)

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
Preconditioning	AEC-Q100#A1	JESD22A113	231 X 3lots	0 fail	Level 3. Prior to TCT, PCT, THB. F/T check before and after at room temp. Delam. on die surface is acceptable if can pass subsequent tests.
TCT (temp cycling)	AEC-Q100#A4	JESD22A104	77 X 3 lots	0 fail	Grade 1 : -65~150℃, 500 cycles. (Or equivalent -55~125℃, 1000 cycles) F/T check before and after at high temp
PCT (autoclave or pressure cooker)	AEC-Q100#A3	JESD22A102	77 X 3 lots	0 fail	121℃/30psia/100%RH. a.168 hrs for LF type, b.It's not applied for laminate based packages. F/T check before and after at room temp
THB (temp humidity bias or HAST)	AEC-Q100#A2	JESD22A101, JESD22A110	77 X 3 lots	0 fail	THB: 85℃/85%RH/1000 hrs with bias HAST: 130℃/85%RH/Minimum 96 hrs with bias (or 110℃/85%RH/264 hrs) F/T check before and after at high temp

Production Reliability Monitoring

1. Philosophy of Reliability Monitoring

In order to guarantee the high standard of reliability for each wafer technology family, a reliability monitoring methodology is executed. By monitoring the data of sampling HTOL yield, RA department will determine if extended burn-in is needed for any specified lots. To screen out any potential failure parts, it is necessary to do 100% extended burn-in for the whole mother lot if the sampling HTOL result is substandard. The reliability monitoring process flow is shown in below Figure. 1.

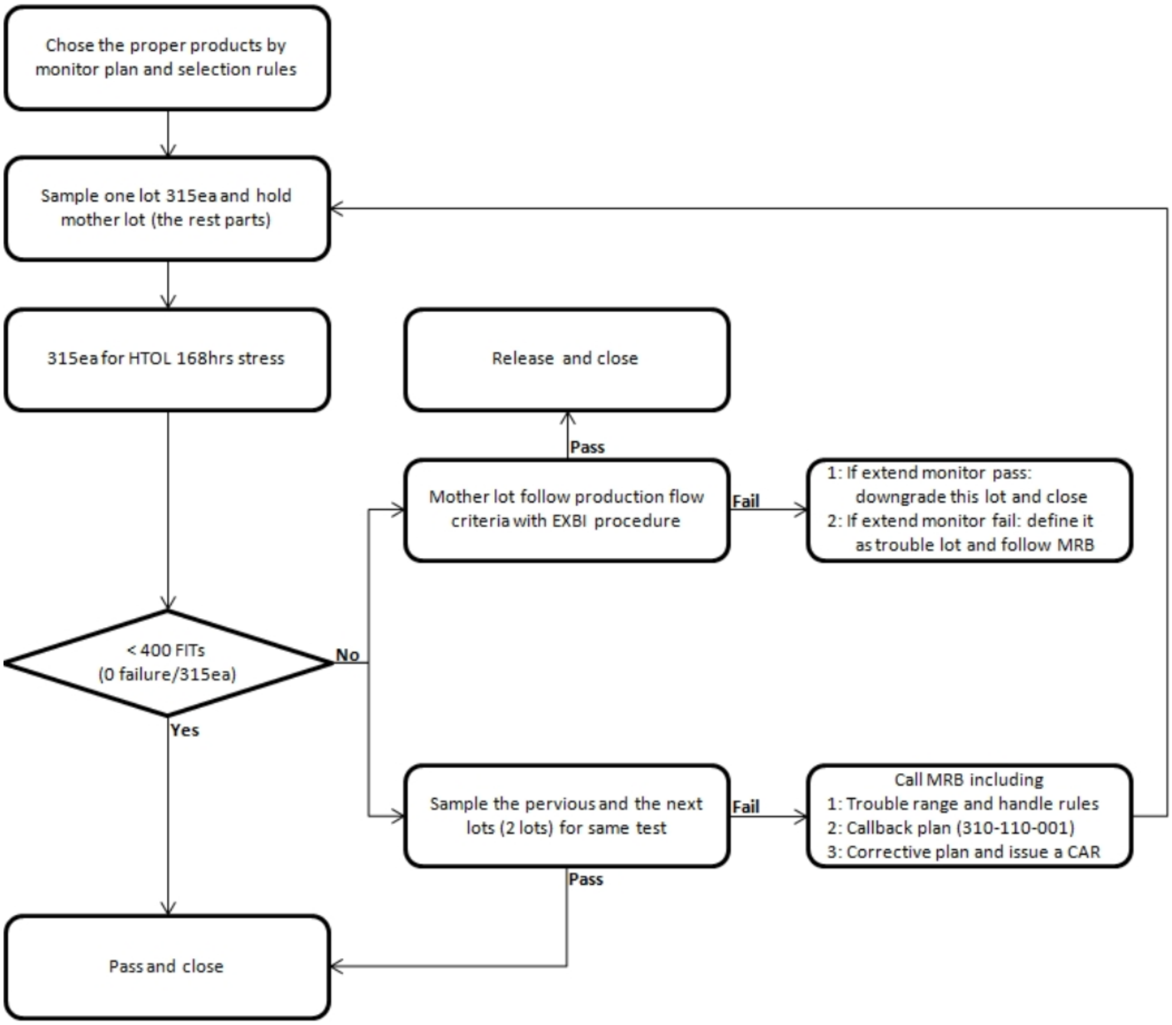
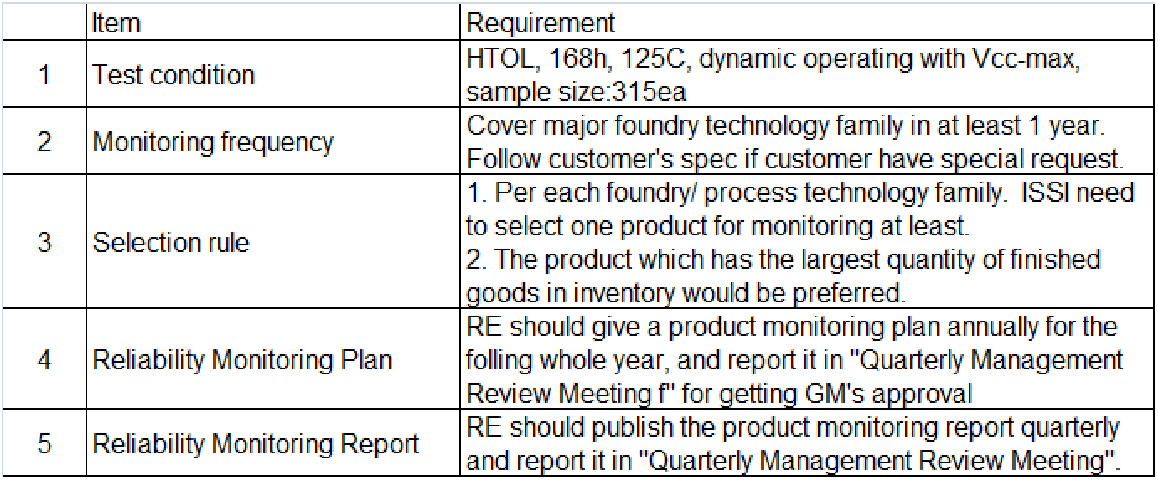


Figure 1 – Reliability Monitor Flow

2. Reliability Monitor Procedure

The Product Reliability Monitoring should be executed following below requirement (See below Table 1). All these topics cover the requirement from the spec of JESD 659 Failure-Mechanism-Driven Reliability Monitoring/ section 6.



	Item	Requirement
1	Test condition	HTOL, 168h, 125C, dynamic operating with Vcc-max, sample size:315ea
2	Monitoring frequency	Cover major foundry technology family in at least 1 year. Follow customer's spec if customer have special request.
3	Selection rule	1. Per each foundry/ process technology family. ISSI need to select one product for monitoring at least. 2. The product which has the largest quantity of finished goods in inventory would be preferred.
4	Reliability Monitoring Plan	RE should give a product monitoring plan annually for the folling whole year, and report it in "Quarterly Management Review Meeting f" for getting GM's approval
5	Reliability Monitoring Report	RE should publish the product monitoring report quarterly and report it in "Quarterly Management Review Meeting".

Table 1: Product Reliability Monitoring Requirement Table

Regarding Flash product, it need to do cycling test before HTOL.

Besides HTOL monitor, ISSI also had performed HTSL monitor.

ISSI Reliability Test conditions

1 Device Related Tests

1.1 High Temperature Operating Life Test

Condition :	Dynamic operation, T = 125 ℃.
Duration :	Up to 1000 hrs, failed device were counted at 168, 500 and 1000hrs
Failures :	When a device fails to pass production test program
Calculation :	Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed.

1.2 Infant Mortality Test

Condition : Dynamic operation, T=125 ℃

Duration : Up to 96 hrs, failed device were counted at 8, 16, 24 and 96 hrs

Failures : When a device fails to pass production test program

Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed

1.3 Electrostatic Discharge (ESD) and Latch-up Tests

ISSI currently performs two types of ESD tests :

1) The Human Body model (HBM), according to ANSI/ESDA/JEDEC JS-001

2) The Charge Device model (CDM), according to ANSI/ESDA/JEDEC JS-002

During the tests, the applied voltage is increased in steps until reaching the maximum passing voltage.

The test sequence for ESD is listed as following:

1) Zap all IO pins (+/-) respectively to VDD and Vss pins.

2) Zap all IO pins (+/-) respectively to all other IO pins.

3) Zap all VDD pins (+/-) respectively to all Vss pins.

4) Zap all VDD pins (+/-) respectively to all other Vdd pins.

Latch-up test: In accordance with JEDEC standard No.78, the currents are injected into the input, output and I/O pins, and Icc is monitored to see whether latch-up has occurred.

The test sequence of latch-up is listed as following:

1) Current trigger to all IO pins (+/-) respectively with all input pins biased during VDD power is applied.

2) Voltage trigger to all VDD pins respectively with all input pins biased during VDD power is applied.

1.4 Soft Error Rate

(JEDEC Standard 89)

Source : Americium 241, with half life = 432.7 ± 0.5 years

Alpha particle activity: 4.948K Bq

Alpha particle flux density: 4.53 x 105 / cm2-hour

Acceleration factor: source α -intensity / package α -intensity.

Example: for molding compound with an emission of 0.001/cm2-hr, the acceleration factor = 4.53x108, Test condition: After de-capsulation, the radioactive source was directly placed over the die surface. Both the source and die were covered to avoid ambient light; Pattern is written into the cell and data are continuously read out. The test arrangement is shown in below Figure 2 ~ 4.

Figure 2 – Radioactive Source: Americium 241

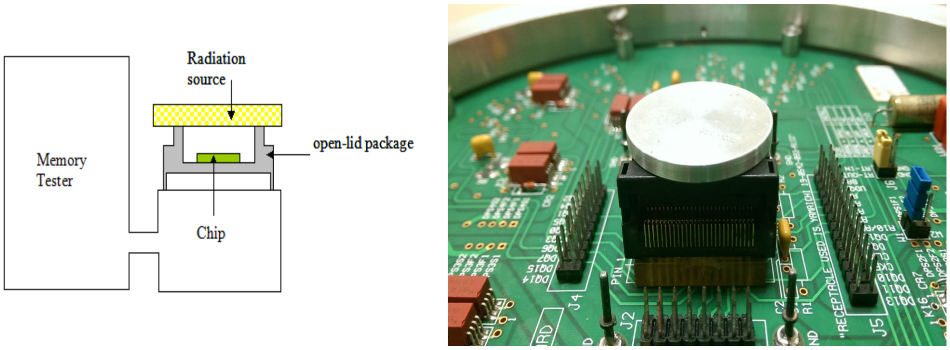


Figure 3 – SER Test Arrangement

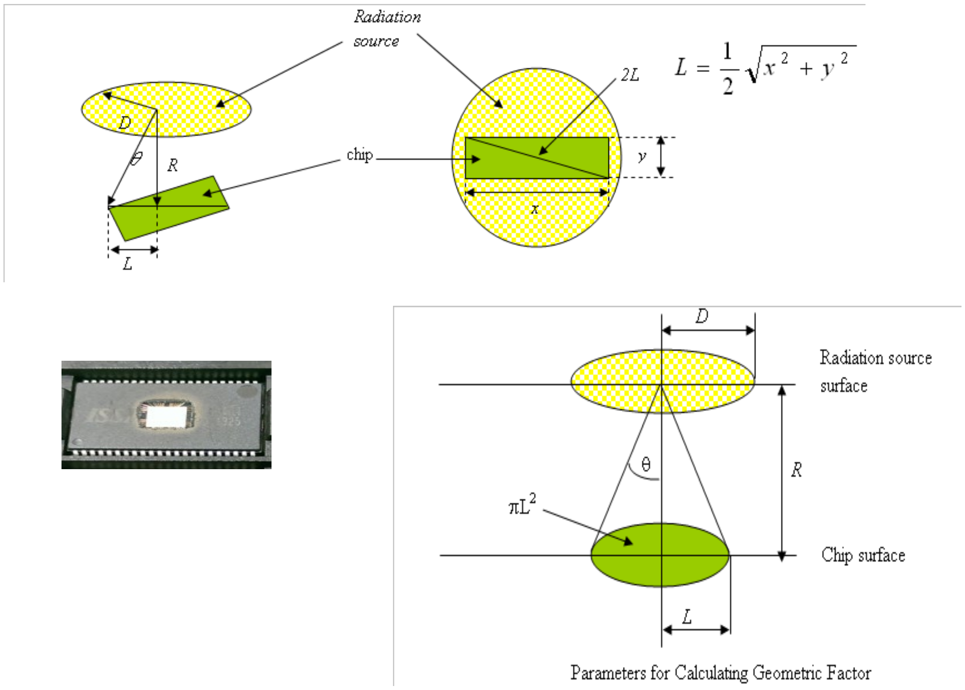


Figure 4 – Geometric Factor about how Alpha from Am source into chip surface

Endurance Cycling and Data Retention tests

(Refer to MIL-STD-883 1033 and JEDEC 22 A117)

ISSI currently performs these two special tests on Flash devices for reliability evaluation.

Endurance Cycling test evaluates the quality of the tunnel oxide of Flash products.

Condition : Continued program-erase operation to cause charge trapping or even breakdown in the tunnel oxide.

Duration : 100K cycles at room temperature and high temperature.
(*Different cycling SPEC refers to datasheet)

Failures : measure threshold shift or cell current that eventually cause failure of a cell to retain data

Calculation : percentage of cells that cannot retain data as a function of program-erase cycling

Data retention test measures the stability of electron in the floating gate of Flash products.

Condition : high temperature(typically, 125 or 150 ℃) with no bias

Duration : 1000 hours

Failures : measure threshold shift or cell current that eventually cause failure of a cell to retain data

Calculation : percentage of cells that cannot retain data after baking

1.6 High Temperature Storage Life Test

A. Condition : , T = 150 ℃.

B. Duration : Up to 1000 hrs.

C. Failures : When a device fails to pass production test program

Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed.

2. Package Related Tests

2.1 Pre-condition Test

Procedure:

1) baking 24 hrs at 125 °C;
2) moisture soaking at certain temperature and humidity level. For level 3: T=30 °C and RH=60%, for 192 hrs;
3) re-flowing solder IR at 240 °C/260 °C for regular and Pb-free packages respectively

2.2 Highly Accelerated Stress Test

Condition : Steady-state temperature humidity bias, voltage is normally set at 1.1× Vccmax, T = 130 °C, 85% RH, 33.3 psi.

Duration: Electrical tests conducted at 96 hrs (or 110°C/85%RH/264 hrs)

Failure: When device fails to pass production test program

Calculation : Both temperature and humidity acceleration factors are considered for the failure rate calculation. Poisson probability distribution with confidence level = 60% is assumed.

2.3 Temperature Cycling Test

Condition: T = -65 to +150 °C temperature cycle, transition period: 5 min.

Duration: Electrical tests conducted after 250 temperature cycles.

Failure: When device fails to pass production test program

Calculation: Poisson probability distribution with confidence level = 60% is assumed.

2.4 Pressure Cooker Test

Condition : No bias, T=121 °C, relative humidity (RH) = 100%, pressure 15 psi.

Duration : Electrical tests conducted at 168 hrs for Non BGA pkg and 96hrs for BGA pkg. (Reference only for BGA)

Failure : When device fails to pass production test program

Calculation : Poisson probability distribution with confidence level = 60% is assumed.

2.5 Pressure Cooker Test

Condition : T = 150 °C.

Duration : Up to 1000 hrs.

Failures : When a device fails to pass production test program

Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed.

ISSI Reliability Test Equipment List

The reliability test equipment utilized throughout ISSI's device measurement laboratory and approved subcontractors are shown in below Table.

Category	Item	Application	Application Site
Visual	Stereo Microscope	For visual inspection of wafer and package parts	In-house lab
	Scanning Electron Microscope (SEM)	Inspect surface or cross section of a device at high magnification	In-house lab
	Acoustic Microscope (CSAM)	For visual inspection delamination in package	In-house lab
	Optical Microscope	For visual inspection both wafer and package parts	In-house lab
	X-ray	To inspect the bonding wire of encapsulated devices	In-house lab
Electrical Test	Keytek ESD & Latch-up Test system	To test ESD and Latch-up, both JEDEC and EIAJ modes available	Currently in subcontractor
	Curve Tracer	To measure parameters	In-house lab
	Parameter Tester	To measure parameters	In-house lab
	Oscilloscope	To test timing and functionalities	In-house lab
	Bench testers (GII, Adventest -Tester, EPRO-142,etc.)	To test parametric and functional characteristics.	In-house lab
	MOSAID Tester	To test functionalities and parameters	In-house lab
Stress Test	Temperature Probe System	To probe the device at high temperature.	In-house lab
	HTOL Oven	To do high-temperature operating life test	In-house lab
	HAST Test System	To do highly accelerative stress test	In-house lab
	Temperature Cycling System	To do temperature cycling test (-65 ℃ to 150 ℃)	In-house lab
	Bake Oven	To do baking and data retention test.	In-house lab
	Temp.& Humid. Storage Chamber	To do high temp and humidity soak test.	In-house lab
	PCT Test System	To do pressure cooker test.	In-house lab
	IR-reflow chamber	To do preconditioning test.	In-house lab
	Other Package Related Tests	To quality the leads, marking, etc.	In-house lab

Figure 1. STK Burn-in Oven, for HTOL test

Figure 2. Signality Burn-in Oven, for HTOL test

Figure 3. HIRAYAMA Pressure Oven, for HAST test

Figure 4. HITACHI Thermal Shock chamber for TCT test

Figure 5. HITACHI Cycling Oven, for TCT test

Figure 6. ISUZU High Temp Oven, for HTS test

Figure 7. HITACHI Humidity Oven, for THS test

Figure 8. KSON Temperature cycle chamber and Keithley system switch/mutimeter, for solder joint life test

Zero Defect Statistics

Process Average Testing (PAT), Statistical Yield Analysis (SYA), and Junction Verification Test (JVT)

To enhance the quality control and achieve the zero defect target for automotive grade parts, we need to implement the PAT, SYA, and JVT concept in the production flow.

1 Part Average Testing (PAT)

1.) Definition:

Part Average Testing (PAT) is intended to identify Components that perform outside the normal statistical distribution.

2.) Purpose:

Every part is built with a particular design and process which, if processed correctly, will yield a certain consistent set of characteristic test results. PAT uses statistical techniques to establish the limits on these test results. These test limits are set up to remove outliers (parts whose parameters are statistically different from the typical part) and should have minimal yield impact on correctly processed parts from a well controlled process.

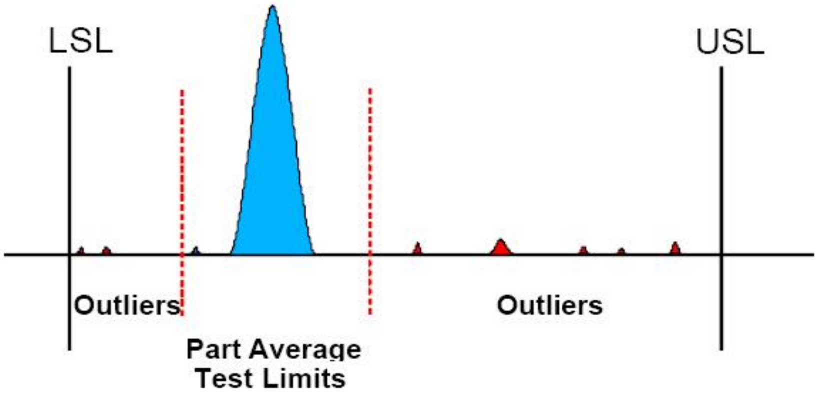


Figure 1 Graphical Representation of Part Average Test Limits and Outliers

History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems.

3.) Method:

a. Setting the Test Limits

PAT Limits = Mean ± 6 sigma

PAT test limits shall not exceed the device specification limits.

Test limits may be set in either a static or dynamic manner. New PAT limits (both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made.

b. Static PAT limits

The static limits are established based on an available amount of test data and used without modification for some period of time.

Sample Size:

Package parts: 30 pass parts × at least 6 lots.

Wafer level: 30 pass dies from at least 5 die located × at least 6 lots.

When data from six lots is not available, data from characterization lots may be used. This data shall be updated as soon as production data is available.

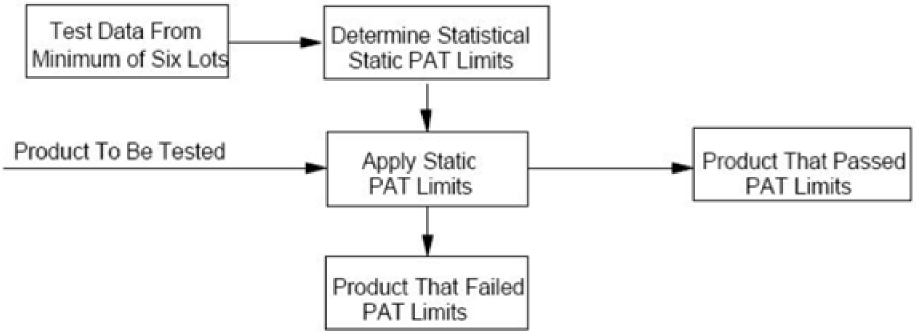


Figure 1 Determining Static PAT Limits

The first 6 months: PAT test limits shall be reviewed and updated as required using current data of production or the last 8 lots. Older data shall not be used.

After 6 months: The static PAT limits shall be reviewed and updated as needed on a quarterly (every 3 month) basis.

c. Dynamic PAT limits

The dynamic test limits are based on the static limits, but are established for each lot and continually change as each lot is tested.

Sample Size: Same as Static PAT limits

The dynamic limits shall not exceed the static limits.

Dynamic PAT can provide tighter limits without causing rejection of good parts because it does not have to consider the lot -to-lot variation that is part of Static PAT Limits.

This analysis establishes new tighter test limits for that particular lot (or wafer) and removes additional outliers.

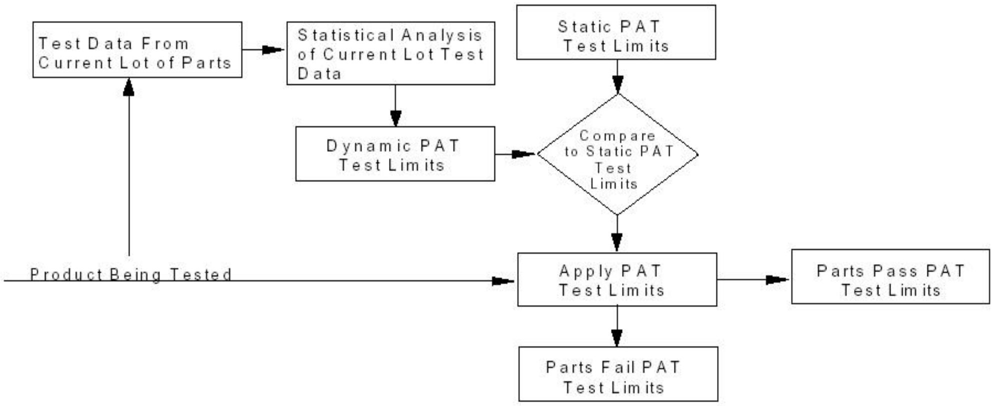


Figure 2 Determining Dynamic PAT Limits

The lot of parts being tested must be held in a manner that allows the outliers to be removed after the test limits for the lot have been calculated and applied.

4.) Application on electrical tests

Any electrical parameter with a Cpk greater than 2.0 (CPK = 2.0 = 6σ) is considered a candidate for implementation.

PAT limits should be used for all electrical tests if possible, but shall be established for at least the important characteristics as below :

a. Junction Verification Test (JVT) - Pin Leakage Test

b. Standby power supply current (IDD or ICC)

c. IDDQ: tested with at least 70% transistor-level coverage (TLC). If the device design is not capable of being tested, then this requirement does not apply.

d. Output breakdown voltage (BVCES or BVDSS)
Output leakage (ICES or IDDS), measured at 80% of the breakdown voltage value
Output current drive (IOUT) and output voltage levels (VOUT)

e. Additional tests:

1) Voltage Stress Test (Vs)

2) Low Level Input Current (IIL)

3) High Level Input Current (IIH)

4) Propagation Delay Or Output Response Time

5) Rise/Fall Times

6) Low Level Output Voltage (VOL)

7) High Level Output Voltage (VOH)

8) Extended Operating Tests

Extended operating tests are tests beyond the device specification requirements intended to increase the effectiveness of PAT. The following are some examples of extended operating tests: a.) voltage stress b.) low voltage operation c.) high voltage operation d.) operating frequencies above specification requirements e.) operating frequencies below specification requirements on power devices, demonstration of safe operating capability at 60% of safe operating limit, followed by leakage testing, etc.

The only restriction on these tests is that it must be demonstrated that the test does not adversely affect the reliability of the part.

2 Statistical Yield Analysis (SYA)

1.) Definition:

Statistical Yield Analysis (SYA) identifies lots of components that yield abnormal distributions, or contain abnormal failure characteristics.

2.) Purpose:

Utilizes statistical techniques to identify a wafer, wafer lot, or component assembly lot that exhibits an unusually low yield or an unusually high bin failure rate. Experience has shown that wafer and component assembly lots exhibiting these abnormal characteristics tend to have generally poor quality and can result insignificant system reliability and quality problems that impact the customer.

3.) Method:

a. 2 ways: statistical yield limits (SYL) and statistical bin limits (SBL) results. Both use test limits based on Part Average Testing (PAT) Limits.

b. Sample Size: Collect data from at least six lots and determine the mean and sigma value for the percentage of devices passing per lot and the percentage of devices failing each bin-out per lot

Early in production of a part, when data from six lots is not available, data from characterization/matrix lots may be used. This data shall be updated as soon as production data is available

c. The first 6 months: This early data shall be reviewed and updated using current data at least every 30 days. The current data used shall include the data available since the last update or at least the last 8 lots. Older data shall not be used

After 6 months: the limits shall be updated on a quarterly (every 3months) basis

d. Setting the value for SYL and SBL

$$SYL_1 = \text{Mean} - 3\ \text{Sigma}$$
$$SBL_1 = \text{Mean} + 3\ \text{Sigma}$$

$$SYL_2 = \text{Mean} - 4\ \text{Sigma}$$
$$SBL_2 = \text{Mean} + 4\ \text{Sigma}$$

e. Disposition: Any lot that fall below SYL1 or exceed SBL1 shall be held for engineering review. In addition, lots that fall below SYL2 or exceed SBL2 may be impounded and require customer notification before release. Analysis shall be performed on failures to determine the failure mechanism causing these abnormal failure rates.

f. Records: The supplier shall maintain records on all lots that fall below SYL1 or exceed SBL1. This data shall include the root cause for the yield problem and corrective action taken to prevent reoccurrence of the problem. It should also include any special testing or screens that were performed on lot and the customer that approved the shipment of the parts in question.

4.) Customer Notification

a. Supplier shall have determined the failure mechanism and, based on his experience, determine the corrective action required to prevent a reoccurrence of the condition in future product. The supplier shall also present a plan for additional tests and screens which could provide the user with reasonable certainty that the product he receives will be at least equal to normal product.

b. The customer reserves the right to reject material that falls below SYL2 or exceeds SBL2 if the supplier data does not satisfy his concerns about the quality. The parts from the lots falling below

SYL2 shall not be supplied to distributors as meeting AEC - Q100 if the supplier does not know who the customer is and customer approval cannot be obtained.

3 Junction Verification Test (JVT)

1.) Definition:

Junction Verification Test (JVT) is also called “Pin leakage Test”. This test will verify that the semiconductor device pins have normal junction characteristics with respect to substrate and with respect to VDD in the case of CMOS components.

2.) Purpose:

Junction Verification Test (JVT) is used to identify IC which have wounded electrical junctions or are susceptible to EOS or a latch up condition and, perform outside the normal statistical distribution.

3.) Method:

Use the following measurement approach to establish the PAT limits for pin leakage.

a. With all pins grounded except the pin under test (PUT):

1. Force -10mA into each pin, measure the forward biased junction voltage (V F1).
2. For CMOS, also force +10mA into each pin, measure the forward biased junction voltage (VF1).
3. Test VDD (VCC) separately with respect to the substrate using -10mA, measure the forward biased junction voltage (VF2).
4. Statistically analyze this data to determine the mean for VF1 and VF2.

b. With all pins grounded except the pin under test (PUT), and using the VF1 and VF2 values determined above, measure the leakage current:

1. Apply -0.8 VF1 (80% of forward bias voltage) to each pin, measure the leakage current.
2. For CMOS, also apply +0.8 VF1 to each pin, measure the leakage currents.
3. Apply -0.8 VF2 to VDD (VCC), measure the leakage current.
4. Statistically analyze this data to determine the leakage current PAT limits.

c. After the conclusion of the final ATE test and following powering down, perform this test method to detect any possible damage that could have occurred during testing.

Environmental Management

As a technology leader, ISSI designs, develops and markets high performance semiconductors throughout the world. ISSI acknowledges our responsibility to manage these functions in a responsible manner, endeavoring to preserve, protect, and whenever possible to enhance the environment. To achieve these goals, we consider and control all key factors which impact the environment including the sourcing of raw materials, manufacturing processes and disposal and recycling of materials. With the continuous effort in pursuing an environmentally friendly product strategy, ISSI became the first design house in Taiwan that achieved the ISO 14001:1996 standard in January 2004 and maintains its ISO14001 certification.

The Environment Management (EM) System defined in ISSI EM Manual is in compliance with the requirements of ISO 14001: 2015. In addition, we also rely on external subcontractors, such as wafer foundries and assembly houses. All of them are required to be ISO 14001-certified. For your reference, please see Technical Documents in the website (for member, password is needed) or contact us directly for copies of ISSI Vendors' ISO 14001 certificates.

Notice:
Part of making dismantling and recycling of ELV and electronics more environmental friendly, please be advised that end-of-life materials are disposed following ELV Directive (end-of-life vehicles regulations, Directive 2000/53/EC) and WEEE Directive (Waste Electrical & Electronic Equipment, Directive 2012/19/EU).

To think about and treat fairly the world we live in ...

Environmental Policy

Integrated Silicon Solution Inc. (ISSI), a technology leader, designs, develops and markets high performance semiconductors throughout the world. ISSI acknowledges our responsibility to manage these functions in a responsible manner, endeavoring to preserve, protect and where possible enhance the environment. To achieve these goals, we consider and control all key factors which impact the environment including the sourcing of raw material and manufacturing processes.

Our vision for the environment is C.L.E.A.N.

Continuous Improvement
Undertake actions to prevent pollution and to maintain, review and continuously improve our environmental management system.
Legal Requirements
Comply with all relevant environmental legislation and regulations.
Environment
Develop, regularly review and achieve environmental objectives, targets and improvement plans.
Awareness
Ensure all are trained and aware of the importance of their environmental responsibilities.
Naturalization

Make the commitment to the environment a natural by-product of our processes and business activities.

All worldwide ISSI locations adhere to ISSI Environmental Policy. As prescribed by the ISO 14001:2015 Standard, ISSI Environmental Policy shall be reviewed to ensure that it:

1) Remains appropriate to the nature, scale, and environmental impacts of the organization's activities, products, or services.
2) Includes a commitment to continual improvement and prevention of pollution.
3) Includes a commitment to comply with relevant environmental legislation and regulations, and with other requirements to which the organization subscribes
4) Provides the framework for setting and reviewing environmental objectives and targets
5) Is documented, implemented, maintained, and communicated to all employees
6) Is available to the public.

2 Environmental Management

The Environment Management (EM) System defined in ISSI EM Manual is in compliance with the requirements of ISO 14001:2015. In addition, we also rely on external subcontractors, such as wafer foundries and assembly houses. All of them are required to be ISO 14001-certified. For your reference, please see Technical Documents in the website (for member, password is needed) or contact us directly for copies of ISSI
vender's ISO 14001 certificates.

2.1 ISO14001 Certificate

With the continuous effort in pursuing an environmentally friendly product strategy, ISSI became the first design house in Taiwan that achieved the ISO 14001:1996 standard in January 2004.

CERTIFICATE

This is to certify that

Integrated Silicon Solution, Inc.
Chingis Technology Corporation

No. 2, Technology Road V, Hsinchu Science Park
Hsinchu
Taiwan

has implemented and maintains an **Environmental Management System**.

Scope:
The environmental activities and supporting processes associated with the design of integrated circuit products.

Through an audit, documented in a report, it was verified that the management system fulfills the requirements of the following standard:

ISO 14001 : 2015

Certificate registration no.	20001373 UM15
Date of revision	2021-07-28
Date of certification	2021-08-08
Valid until	2024-08-07

DQS Inc.

Brad McGuire

Brad McGuire
Managing Director

Accredited Body: DQS Inc., 1500 McConnor Parkway, Suite 400, Schaumburg, IL 60173 USA
Administrative Office: DQS Taiwan Inc., 8F, 23, Yuan Huan West Road, Feng Yuan Dist.,
Taichung City, Taiwan 420

2.2 Environmental Management Organization

ISSI Environmental Management organization is outlined as Figure 1.

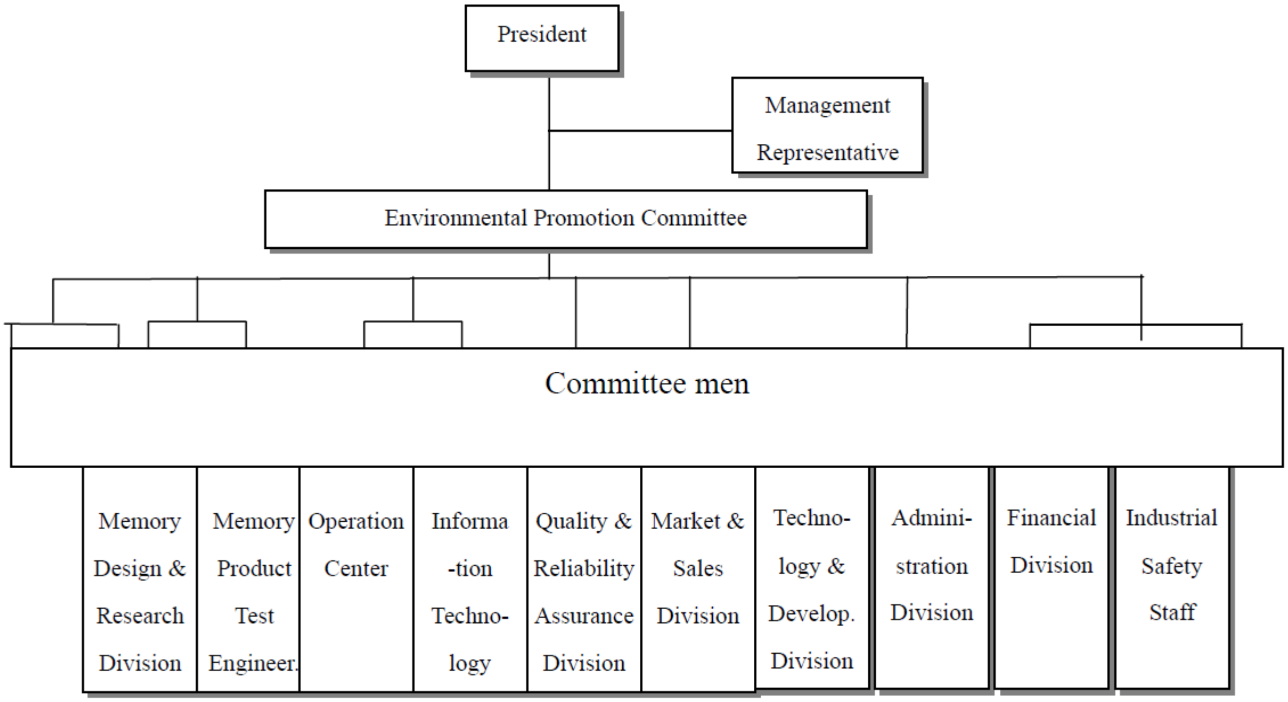


Figure 5-2. ISSI EM Organization

3 Environmental Substances Management

Through continuous improvement, ISSI has positioned itself to be an environmental- friendly enterprise and a green partner of all environment-concerned companies with which ISSI has a business relationship.

3.1 Legislation and SONY Policy

1). Europe – 1 July 2006
Total abolition of Lead, Mercury, Cadmium, Hexavalent Chromium, PFOS, PBB and PBDE has been observed since July 2006, according to the second draft of European Union order (RoHS and WEEE) for the abolishing electrical and electronic equipment.

2). Management Standards for the Restrictively Used Substances (SONY SS-00259)

Table 5-1 List of “Environment-related Substances to be Controlled”

No	Material/Substance Category		ISSI Threshold
1	Heavy Metals 重金屬	Cadmium(Cd)/Cadmium compounds 鎘及其化合物	5 ppm for resin (rubber, film), coatings, inks pigments, dyes.
			Less than 20ppm for lead free solder -Bar solder -Wire solder -Resin flux cored solder -Solder paste ,Solder ball -Soldered sections of purchased PC boards -Component solder
			Less than 75 ppm for homogeneous material
		Lead (Pb)/Lead compounds 鉛及其化合物	100 ppm or less in plastics/inks
			Less than 800 ppm of total in homogenous material
			Less than 500 ppm for lead free solder -Bar solder -Wire solder -Resin flux cored solder -Solder Paste -Solder ball
		Mercury (Hg)/Mercury compounds 汞及其化合物	Less than 1000 ppm of total in homogenous material
		Hexavalent Chromium(Cr6+)/It's compounds 六價鉻及其化合物	Less than 1000 ppm of total in homogenous material
2	Brominated organic compounds 有機溴化合物	Polybrominated Biphenyls (PBBs) 多溴聯苯	<1000ppm or less; Non-detected or intentionally added
		Polybrominated Diphenylethers (PBDEs) Included DecaBDE 多溴聯苯醚	<1000ppm or less; Non-detected or intentionally added
		Hexabromocyclododecane (HBCDD) 六溴環十二烷	Not intentionally added or Max. 0.01wt % (100 ppm) of article even contained as impurities.
	Brominated flame retardants (BFR) 溴系阻燃劑	Other Brominated organic compounds 其他有機溴化合物	Non-detected or intentionally added
3	Chlorinated organic compounds 有機氯化合物	Polychlorinated Biphenyls (PCBs) 多氯聯苯	Not intentionally added
		Polychlorinated naphthalenes (PCNs) 多氯萘	Not intentionally added
		Chlorinated Paraffins (CP) 氯化石蠟	Non-detected or intentionally added
		Polychlorinated Terphenyls (PCTs) 多氯三聯苯	50ppm in material
		Short Chain Chlorlnated Paraffins (C10-C13) 短鏈氯化石蠟	Non-detected or intentionally added, mix, or production of substance in the manufacturing process. Less than 1000ppm of article
	Chlorinated flame retardants (CFR) 氯系阻燃劑	Other Chlorinated organic compounds	Non-detected or intentionally added
4	Halogen 鹵素	Cl, Br.	Must be lower than 900 ppm, respectively, and total amount of PPM must be lower than 1500 ppm (Br + Cl < 1500 ppm).
5	Phthalates 鄰苯二甲酸酯類	Benzyl butyl phthalate(BBP) Dibutyl phthalate(DBP) Bis(2-ethylhexyl)phthalate(DEHP) Diisobutyl phthalate(DIBP)	Less than 1000 ppm of each in homogenous material

6	Organic tin compounds 有機錫化合物	Tributyltin(TBT) compounds 三丁基錫化合物 Triphenyltin(TPT) compounds 三苯基錫化合物 Tributyl Tin Oxide (TBTO) 氧化三丁錫 Dibutyltin(DBT) compounds 二丁基氧化錫 Dioctyltin(DOT) compounds 氧化二辛基錫	Not intentionally added or 0.1wt% (1000ppm) of the article
7	Phosphorous-based Flame Retardants 磷系阻燃劑	Tris(2-chloroethyl) phosphate (TCEP) 磷酸三(2-氯乙基) 酯 Tris (2-chloro-1-methylethyl) phosphate (TCPP) 磷酸三(1-氯丙基) 酯 Tris(1,3-dichloro-2-propyl) phosphate (TDCPP) 磷酸三(1,3-二氯丙基) 酯 Trixylyl phosphate (TXP) 磷酸三(二甲苯)酯	0.1wt% (1000ppm) of the article
8	Asbestos 石棉		Non-detected or intentionally added
9	Specific aze compounds (Certain Azocourants and Azodyes) 特定偶氮化合物		Non-detected or intentionally added
10	Polyvinyl Chloride (PVC) and PVC blends 聚氯乙烯及聚氯乙烯混合物		Not intentionally added or 0.1wt% (1000ppm) of the product *3 Tube is not applicable, since PVC is the main material.
11	Beryllium oxide 氧化鈹 Beryllium copper 鈹青銅		Non-detected or intentionally added.
12	Specific phthalates 特定鄰苯二甲酸鹽	- Diisononyl phthalate(DINP, 68515-48-0, 28553-12-0) - Di-isodecyl phthalate(DIDP, 68515-49-1, 26761-40-0) - Di-n-octyl phthalate(DnOP, 117-84-0) - Di-n-hexyl phthalate(DnHP, 84-75-3) - Bis(2-methoxyethyl) phthalate(DMEP, 117-82-8) - Di-iso-pentyl phthalate(DIPP, 605-50-5) - n-Pentyl-isopentyl phthalate(nPIPP, 776297-69-9) - Di-n-pentyl phthalate(DnPP, 131-18-0) - Diethyl phthalate(DEP, 84-66-2) - Dimethyl phthalate(DMP, 131-11-3) - 1,2-Benzenedicarboxylic acid, di-C6-8-branched alkyl esters, C7-rich(DIHP, 71888-89-6) - 1,2-Benzenedicarboxylic acid, di-C7-11-branched and linear alkyl esters(DHNUP,68515-42-4) - 1,2-Benzenedicarboxylic acid, dipentylester, branched and linear(DPP, 84777-06-0)	Non-detected or intentionally added

13	Hydrofluorocarbon (HFC) , Perfluorocarbon (PFC) 氫氟碳化合物(HFC) , 全氟化碳 (PFC)		Non-detected or intentionally added
14	PFOS & PFOA 全氟辛烷硫酸 & 全氟辛酸		Non-detected or intentionally added 0.1wt %(1000 ppm) by weight in material.
15	Ozone Delpting Substances 臭氧危害物質		Banned and must not be used when manufacturing parts and device.
16	Radioactive Substances 放射性物質		Banned and must not be used when manufacturing parts and device.
17	Cobalt dichloride 二氯化鈷	Pneumatic panels to indicate water contamination	Not intentionally added in Moisture indicator used for a desiccant agent (e.g. silica gel) 0.1wt%(1000ppm) of article
18	Specific benzotriazole 特定苯并三氮唑		Non-detected or intentionally added
19	Bisphenol A 雙酚 A		Not intentionally added or <0.1wt% (SVHC)
20	Dimethyl fumarate(DMF) 富馬酸二甲酯		Non-detected or intentionally added
21	PAHs 多環芳香烴		Non-detected (MDL: < 0.2mg/kg) in toy which contact with skin and for the baby.
22	REACH SVHC substances 高關注物質	Refer to ECHA candidate list :https://echa.europa.eu/candidate-list-table	< 0.1wt % of the article

Note:

1) Due to restrictions in manufacturing technologies, the lead concentration found in the electroplating of IC’s outer leads may be exempt from the threshold level (100 PPM). But the lead concentration must still not exceed 1000 PPM. Assembly house must control lead concentration lower than 800 ppm while Plating process and measurement in process monitor to avoid any deviation.
2) For Cabolt dichloride must be prohibited from Dec-01st '2008.
3) Sony Class III definition: No deadline for banning the use is currently set for the substances classified into this level. They shall be classified into Level 2 to be banned in phases, Depending on the availability of alternative parts and material that satisfy the intended application.
4) Non-detected level please follow the MDL(Method Detect Limit) by third party test report.

3.2 Green Partner Certification

The environment-related substances shown in Table 5-1 above are controlled in the Green Partner (GP) rule. These controlled substances will be phased out gradually in ISSI depending on specific schedule in GP rule defined by customer, although the final regulation about environmental conscious substances has not been integrated in the world, like EU, Japan and US yet.

ISSI has been very proactive in the promotion of environmental-friendly products. After much effort on surveying the substance used in our packages, we have learnt the content of these substances quite well and conveyed the information to our customers. As a result, ISSI was first awarded as SONY's Green Partner in June 2003 and got renewed again per two years. Renewal of 2013 version is done. ISSI also was awarded Canon's Certificate of Green Activity. The current SONY certificate number is shown in Table 5-2 and Canon certificate number is shown in Table 5-3.

【Certification No,】	【Factory Name】	【Valid date】
FC005567	Integrated Silicon Solution,Inc. (ISSI)	03/31/2020
FC005569	Integrated Silicon Solution, Inc. (ICSI)	03/31/2020

Table 5-2 SONY Green Partner certificate

【Certification No】	【Partner Code】	【Company Name】	【Valid date】	【Place】
3914	M050（Marubun）	Integrated Silicon Solution, Inc	Dec-2020	Taiwan/ Headquarters

Table 5-3 Canon Green certificate

3.3 Industry Definition of Lead-free & Halogen-free

1) Lead-free package :

Pb content in individual material must be less than the limited level

- IPC/JEDEC	: Pb < 2000 ppm
- EU(ST/Philip/Infineon)	Pb < 1000 ppm-
- JEITA	Pb < 1000 ppm
- ISSI	**Pb < 800 ppm**

2) Halogen-free package:

In addition to the requirement of Pb-free package, the Halogen-free package must reduce the content of halogen and antimony trioxide[3] to the minimum level

- Japan Electronic Insulating Material Association:	
	Br, Cl, Sb < 900 ppm, respectively
- ST/Philip/Infineon	Halogen (Br + Cl) < 900 ppm
	based on JPCA-ES-01-1999
- ISSI	**Br, Cl, Sb < 900 ppm, respectively**
	Halogen (Br + Cl) < 1500 ppm

The new ‘Green’ definition will be followed and updated with the green standard of the environmental concerned substances changing around the world.

3) Future Material declaration requirement at an Article level for EU/REACH (Registration, Evaluation, Authorization and Restriction of Chemicals) The European Chemicals Agency (ECHA) has published the candidate list of substances of very high concern (SVHC) from 28 October 2008. ISSI will notify customer in case of ISSI use and exceed threshold level (if >0.1 % w/w) in the future once a new candidate list of REACH which is demanded by ECHA. The SVHC substances please refer to ECHA candidate list: https://echa.europa.eu/candidate-list-table

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[3] Even though antimony is not a halogen element, it is often used with halogen in the flame retardant of the molding compound. We follow ASE (Advanced Semiconductor Engineering) Group’s convention to include antimony trioxide as a “halogen” element in the category of “halogen-free” package.

* All refractory ceramic fibers are covered by index number 650-017-00-8 in Annex VI of the so-called CLP regulation - Regulation No 1272/2008 on the classification, labeling and packaging (CLP) of chemical substances.

No.	Substance Name	CAS No.
1	三乙基砷酸酯 Triethyl arsenate	15606-95-8
2	蒽 Anthracene	120-12-7
3	4,4'- 二氨基二苯甲烷 4,4'- Diaminodiphenylmethane(MDA)	101-77-9
4	鄰苯二甲酸二丁酯 Dibutyl phthalate(DBP)	84-74-2
5	氯化鈷 Cobalt dichloride	7646-79-9
6	五氧化二砷 Diarsenic Pentaoxide	1303-28-2
7	三氧化二砷 Diarsenic trioxide	1327-53-3
8	重鉻酸鈉·二倍結晶水 Sodium Dichromate	7789-12-0 10588-01-9
9	5-叔丁基-2,4,6-三硝基間二甲苯 5-tert-butyl-2,4,6-trinitro-m-xylene(musk xylene)	81-15-2
10	鄰苯二甲酸二(2-乙基已基)酯 Bis(2-ethylhexyl) Phthalate (DEHP)	117-81-7
11	六溴環十二烷 Hexabromocyclododecane(HBCDD) and all major diastereois	134237-50-6 134237-52-8 134237-51-7
12	短鏈氯化路蠟 Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins)	85535-84-8
13	氧化三丁錫 Bis(tributyltin)oxide (TBTO)	56-35-9
14	砷酸氫鉛 Lead hydrogen arsenate	7784-40-9
15	鄰苯二甲酸丁酯苯甲酯 Benzyl butyl phthalate (BBP)	85-68-7
16	蒽油 Anthracene oil	90640-80-5
17	蒽油，蒽糊，輕油 Anthracene oil, anthracene paste, distn. Lights*	91995-17-4
18	蒽油，蒽糊，蒽餾分離液 Anthracene oil, anthracene paste, anthracene fraction	91995-15-2
19	蒽油，含蒽量少 Anthracene oil, anthracene-low	90640-82-7
20	蒽油，蒽糊 Anthracene oil, anthracene paste	90640-81-6
21	煤瀝青，高溫 Coal tar pitch, high tempperature	65996-93-2
22	丙烯醯胺 Acrylamide	79-06-1
23	矽酸鋁，陶瓷耐火纖維 Aluminiosillcate, Refractory Ceramic Fibres	None
24	矽酸鋁氧化鋯，陶瓷耐火纖維 Zirconia Aluminosilicate, Refractor Ceramic Fibres	None
25	2,4 二硝基甲苯 2,4-Dinitrotoluene	121-14-2
26	鄰苯二甲酸二異丁酯 Dilsobutyl phthalate	84-69-5
27	鉻酸鉛 Lead chromate	7758-97-6
28	紅色鉬鉻酸硫酸鹽 Lead chromate molybdate sulphate red (C.I. Pigment Red 104)	12656-85-8
29	黃色硫化鉻酸鉛 Lead sulfochromate yellow (C.I. Pigment Yellow 34)	1344-37-2
30	三 2-(氯乙基)磷酸酯 Tris (2-chloroethyl) phosphate	115-96-8
31	三氯乙烯 Trichloroethylene	79-01-6
32	硼酸 Boric acid	10043-35-3 11113-50-1
33	無水四硼酸二鈉 Disodium tetraborate, anhydrous	1303-96-4 1330-43-4 12179-04-3

34	水合七氧四硼酸二鈉 Tetraboron disodium heptaoxide, hydrate	12267-73-1
35	鉻酸鈉 Sodium chromate	7775-11-3
36	鉻酸鉀 Potassium chromate	7789-00-6
37	重鉻酸銨 Ammonium dichromate	7789-09-5
38	重鉻酸 Potassium dichromate	7778-50-9
39	硫酸鈷 Cobalt sulfate	10124-43-3
40	硝酸鈷 Cobalt dinitrate	10141-05-6
41	碳酸鈷 Cobalt carbonate	513-79-1
42	醋酸鈷 Cobalt diacetate	71-48-7
43	2-甲氧基乙醇 2-Methoxyethanol	109-86-4
44	2-乙氧基乙醇 2-Ethoxyethanol	110-80-5
45	三氧化鉻 Chromium trioxide	1333-82-0
46	三氧化二鉻 Chromic acid/重鉻酸 Dichromic acid	7738-94-5 13530-68-2
47	乙酸-2-乙氧基乙酯 2-ethoxyethyl acetate	111-15-9
48	鉻酸鍶 Strontium chromate	7789-06-2
49	鄰苯二甲酸二(C7-11 支鏈與直鏈)烷基酯 1,2-Benzenedicarboxylic acid, di-C7-11-branched and linear alkyl esters (DHNUP)	68515-42-4
50	肼 Hydrazine	302-01-2 7803-57-8
51	N-甲基吡咯烷酮 1-methyl-2-pyrrolidone	872-50-4
52	1，2，3-三氯丙烷 1,2,3-trichloropropane	96-18-4
53	鄰苯二甲酸二 C6-8 支链 烷基酯 1,2-Benzenedicarboxylic acid, di-C6-8-branched alkyl esters, C7-rich (DIHP)	71888-89-6
54	鉻酸鉻 Dichromium tris(chromate)	24613-89-6
55	氫氧化鉻酸鋅鉀 Potassium hydroxyoctaoxodizincatedi-chromate	11103-86-9
56	C.I.顏料黃 36 Pentazinc chromate octahydroxide	49663-84-5
57	甲醛和苯胺聚合物 Formaldehyde, oligomeric reaction products with aniline (technical MDA)	25214-70-4
58	鄰苯二甲酸二甲氧乙酯 Bis(2-methoxyethyl) phthalate	117-82-8
59	2-Methoxyaniline; o-Anisidine	90-04-0
60	鄰甲氧基苯胺 4-(1,1,3,3-tetramethylbutyl)phenol, (4-tert-Octylphenol)	140-66-9
61	1,2-二氯乙烷 1,2-Dichloroethane	107-06-2
62	二甘醇二甲醚 Bis(2-methoxyethyl) ether	111-96-6
63	砷酸 Arsenic acid	7778-39-4
64	砷酸鈣 Calcium arsenate	7778-44-1
65	砷酸鉛 Trilead diarsenate	3687-31-8
66	N,N-二甲基乙醯胺 N,N-dimethylacetamide (DMAC)	127-19-5
67	4,4'-二氨基-2,2'-二氯二苯甲烷, 2,2'-dichloro-4,4'-methylenedianiline (MOCA)	101-14-4

68	酚酞 Phenolphthalein	77-09-8
69	疊氮化鉛 Lead azide Lead diazide	13424-46-9
70	收斂酸鉛 Lead styphnate	15245-44-0
71	苦味酸鉛 Lead dipicrate	6477-64-1
72	三甘醇二甲醚 1,2-bis(2-methoxyethoxy)ethane (TEGDME; triglyme)	112-49-2
73	乙二醇二甲醚 1,2-dimethoxyethane; ethylene glycol dimethyl ether (EGDME)	110-71-4
74	α,α-二[(二甲氨基)苯基]-4-甲氨基苯甲醇 4,4'-bis(dimethylamino)-4''-(methylamino)trityl alcohol	561-41-1
75	4'-二(N,N-二甲氨基)二苯甲酮 4,4'-bis(dimethylamino)benzophenone (Michler’s ketone)	90-94-8
76	结晶紫 [4-[4,4'-bis(dimethylamino) benzhydrylidene]cyclohexa-2,5-dien-1-ylidene]dimethylammonium chloride (C.I. Basic Violet 3)	548-62-9
77	碱性蓝 26; 维多利亞藍 B [4-[[4-anilino-1-naphthyl][4-(dimethylamino)phenyl]methylene]cyclohexa-2,5-dien-1-ylidene] dimethylammonium chloride (C.I. Basic Blue 26)	2580-56-5
78	三氧化二硼 (無水硼酸) Diboron trioxide	1303-86-2
79	氨基甲醛 Formamide	75-12-7
80	甲基磺酸铅 Lead(II) bis(methanesulfonate)	17570-76-2
81	N,N,N'N'-四甲基-4,4'-二氨基二苯甲烷 N,N,N',N'-tetramethyl-4,4'-methylenedianiline (Michler’s base)	101-61-1
82	1,3,5-三缩水甘油-S-三嗪三酮 TGIC (1,3,5-tris(oxiranylmethyl)-1,3,5-triazine-2,4,6(1H,3H,5H)-trione)	2451-62-9
83	A,A-二[4-(二甲氨基)苯基]-4-苯基氨基-1-萘甲醇 α,α-Bis[4-(dimethylamino)phenyl]-4 (phenylamino)naphthalene-1-methanol (C.I. Solvent Blue 4)	6786-83-0
84	β-TGIC (1,3,5-tris[(2S and 2R)-2,3-epoxypropyl]-1,3,5-triazine-2,4,6-(1H,3H,5H)-trione) 异氰脲酸 B-三缩水甘油酯	59653-74-6
85	十溴聯苯醚 Bis(pentabromophenyl) ether (DecaBDE)	1163-19-5
86	全氟十三酸 Pentacosafluorotridecanoic acid	72629-94-8
87	全氟十二烷酸 Tricosafluorododecanoic acid	307-55-1
88	全氟十一烷酸 Henicosafluoroundecanoic acid	2058-94-8
89	全氟代十四酸 Heptacosafluorotetradecanoic acid	376-06-7
90	辛基酚聚醚-9，包括界定明確的物質以及 UVCB 物質、聚合物和同系物 4-(1,1,3,3-tetramethylbutyl)phenol, ethoxylated - covering well-defined substances and UVCB substances, polymers and homologues	-
91	分支或線性的壬基酚，含有線性或分支、共價綁定苯酚的 9 個碳烷基鏈的物質，包括 UVCB 物質以及任何含有獨立或組合的界定明確的同分異構體的物質 4-Nonylphenol, branched and linear - substances with a linear and/or branched alkyl chain with a carbon number of 9 covalently bound in position 4 to phenol, covering also UVCB- and well-defined substances which include any of the individual isomers or a combination thereof	-
92	偶氮二甲醯胺 Diazene-1,2-dicarboxamide (C,C'-azodi(formamide))	123-77-3
93	順環己烷-1,2-二羧酸酐 Cyclohexane-1,2-dicarboxylic anhydride (Hexahydrophthalic anhydride - HHPA)	85-42-7

94	甲基六氫苯酐、4-甲基六氫苯酐、甲基六氫化鄰苯二甲酸酐、3-甲基六氫苯二甲酯酐 Hexahydromethylphathalic anhydride, Hexahydro-4-methylphathalic anhydride, Hexahydro-1-methylphathalic anhydride, Hexahydro-3-methylphathalic anhydride	25550-51-0, 19438-60-9, 48122-14-1, 57110-29-9
95	甲氧基乙酸 Methoxy acetic acid	625-45-6
96	1，2-苯二羧二戊酯（支鏈和直鏈） 1,2-Benzenedicarboxylic acid, dipentylester, branched and linear	84777-06-0
97	鄰苯二甲酸二異戊酯 Diisopentylphthalate (DIPP)	605-50-5
98	鄰苯二甲酸正戊基異戊基酯 N-pentyl-isopentylphtalate	-
99	乙二醇二乙醚 1,2-Diethoxyethane	629-14-1
100	N,N-二甲基甲醯胺 N,N-dimethylformamide; dimethyl formamide	68-12-2
101	二丁基錫 Dibutyltin dichloride (DBT)	683-18-1
102	堿式乙酸鉛 Acetic acid, lead salt, basic	51404-69-4
103	堿式碳酸鉛 Basic lead carbonate (trilead bis(carbonate)dihydroxide)	1319-46-6
104	堿式硫酸鉛 Lead oxide sulfate (basic lead sulfate)	12036-76-9
105	二鹽基鄰苯二甲酸鉛[Phthalato(2-)]dioxotrilead (dibasic lead phthalate)	69011-06-9
106	雙(十八酸基)二氧代三鉛 Dioxobis(stearato)trilead	12578-12-0
107	C16-18-脂肪酸鉛鹽 Fatty acids, C16-18, lead salts	91031-62-8
108	氟硼酸鉛 Lead bis(tetrafluoroborate)	13814-96-5
109	氨基氰鉛鹽 Lead cynamidate	20837-86-9
110	硝酸鉛 Lead dinitrate	10099-74-8
111	氧化鉛 Lead oxide (lead monoxide)	1317-36-8
112	四氧化三鉛 Lead tetroxide (orange lead)	1314-41-6
113	鈦酸鉛 Lead titanium trioxide	12060-00-3
114	鈦酸鉛鋯 Lead Titanium Zirconium Oxide	12626-81-2
115	氧化鉛與硫酸鉛的複合物 Pentalead tetraoxide sulphate	12065-90-6
116	顏料黃 41 Pyrochlore, antimony lead yellow	8012-00-8
117	摻雜鉛的矽酸鋇 Silicic acid, barium salt, lead-doped	68784-75-8
118	矽酸鉛 Silicic acid, lead salt	11120-22-2
119	亞硫酸鉛（II）Sulfurous acid, lead salt, dibasic	62229-08-7
120	四乙基鉛 Tetraethyllead	78-00-2
121	三堿式硫酸鉛 Tetralead trioxide sulphate	12202-17-4
122	磷酸氧化鉛 Trilead dioxide phosphonate	12141-20-7
123	呋喃 Furan	110-00-9
124	環氧丙烷 Propylene oxide; 1,2-epoxypropane; methyloxirane	75-56-9
125	硫酸二乙酯 Diethyl sulphate	64-67-5
126	硫酸二甲酯 Dimethyl sulphate	77-78-1
127	3-乙基-2-甲基-2-(3-甲基丁基)噁唑烷 3-ethyl-2-methyl-2-(3-methylbutyl)-1,3-oxazolidine	143860-04-2
128	地樂酚 Dinoseb	88-85-7

129	4,4'-二氨基-3,3'-二甲基二苯甲烷 4,4'-methylenedi-o-toluidine	838-88-0
130	4,4'-二氨基二苯醚 4,4'-oxydianiline and its salts	101-80-4
131	4-胺基偶氮苯 4-Aminoazobenzene; 4-Phenylazoaniline	60-09-3
132	2,4-二氨基甲苯 4-methyl-m-phenylenediamine (2,4-toluene-diamine)	95-80-7
133	6-甲氧基 -間-甲苯胺 甲苯胺 6-methoxy-m-toluidine (p-cresidine)	120-71-8
134	4-氨基聯苯 Biphenyl-4-ylamine	92-67-1
135	鄰氨基偶氮甲苯 o-aminoazotoluene	97-56-3
136	鄰甲基苯胺 o-Toluidine; 2-Aminotoluene	95-53-4
137	N-甲基乙酰胺 N-methylacetamide	79-16-3
138	溴代正丙烷 1-bromopropane; n-propyl bromide	106-94-5
139	鎘 Cadmium	7440-43-9
140	氧化鎘 Cadmium oxide	1306-19-0
141	鄰苯二甲酸二戊酯 Dipentyl phthalate (DPP)	131-18-0
142	分支或線性的乙氧化壬基酚，包括含有 9 個碳烷基鏈的所有獨立的同分異構體和所有含有線性或分支 9 個碳烷基鏈的 UVCB 物質 4-Nonylphenol, branched and linear, ethoxylated [substances with a linear and/or branched alkyl chain with a carbon number of 9 covalently bound in position 4 to phenol, ethoxylated covering UVCB- and well-defined substances, polymers and homologues, which include any of the individual isomers and/or combinations thereof]	-
143	全氟辛酸銨 Ammonium pentadecafluorooctanoate (APFO)	3825-26-1
144	全氟辛酸 Pentadecafluorooctanoic acid (PFOA)	335-67-1
145	硫化鎘 Cadmium sulphide	215-147-8
146	鄰苯二甲酸二己酯 Dihexyl phthalate	201-559-5
147	直接紅 28 Disodium 3,3'-[[1,1'-biphenyl]-4,4'-diylbis(azo)]bis(4-aminonaphthalene-1-sulphonate) (C.I. Direct Red 28)	209-358-4
148	直接黑 38 Disodium 4-amino-3-[[4'-[(2,4-diaminophenyl)azo][1,1'-biphenyl]-4-yl]azo] -5-hydroxy-6-(phenylazo)naphthalene-2,7-disulphonate (C.I. Direct Black 38)	217-710-3
149	亞乙基硫脲 Imidazolidine-2-thione; 2-imidazoline-2-thiol	202-506-9
150	醋酸鉛 Lead di (acetate)	206-104-4
151	磷酸三（二甲苯）酯 Trixylyl phosphate	246-677-8
152	鄰苯二甲酸二己酯（支鏈和直鏈）1,2-Benzenedicarboxylic acid, dihexyl ester,branched and linear	68515-50-4
153	氯化鎘 Cadmium chloride	10108-64-2
154	過硼酸鈉 Sodium perborate; perboric acid, sodium salt	-
155	過氧偏硼酸鈉 Sodium peroxometaborate	7632-04-4
156	2-(2’-羥基-3’,5’-二-叔-戊基苯基)苯並三唑 (紫外線吸收劑 328) 2-(2H-benzotriazol-2-yl)-4,6-ditertpentylphenol (UV-328)	25973-55-1
157	2-[2-羥基-3’,5’-二-叔-丁基苯基]-苯並三唑 (紫外線吸收劑 320) 2-benzotriazol-2-yl-4,6-di-tert-butylphenol (UV-320)	3846-71-7
158	二正辛基-双（2-乙基己基巯基乙酸酯）錫 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (DOTE)	15571-58-1

159	氟化镉 Cadmium fluoride	7790-79-6
160	硫酸鎘 Cadmium sulphate	10124-36-4; 31119-53-6
161	二正辛基-双（2-乙基己基巯基乙酸酯）錫和單辛基-三(2-乙基己基巯基乙酸酯）錫的反應物 Reaction mass of 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate and 2-ethylhexyl 10-ethyl-4-[[2-[(2-ethylhexyl)oxy]-2-oxoethyl]thio]-4-octyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (reaction mass of DOTE and MOTE)	-
162	鄰苯二甲酸二(C6-C6)烷基酯：(癸基，己基，辛基)酯與 1，2-鄰苯二甲酸的複合物且鄰苯二甲酸二己酯含量≥0.3% 1,2-benzenedicarboxylic acid, di-C6-10-alkyl esters; 1,2-benzenedicarboxylic acid, mixed decyl and hexyl and octyl diesters with ≥ 0.3% of dihexyl phthalate (EC No. 201-559-5)	68515-51-5 68648-93-1
163	5-仲丁基-2-（2,4-二甲基環丁-3-烯-1-基）-5-甲基-1,3-二惡烷[1]，5-仲丁基-2-（4,6-二甲基環己-3-烯-1-基）-5-甲基-1,3-二惡烷[2] [覆蓋任何[1]和[2]或者其任意組合的單獨的異構體 (卡拉花醛及其同分易構物) 5-sec-butyl-2-(2,4-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [1], 5-sec-butyl-2-(4,6-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [2] [covering any of the individual stereoisomers of [1] and [2] or any combination thereof]	-
164	硝苯 Nitrobenzene	98-95-3
165	2,4-貳三級丁基-6-(5-氯苯三唑-2-基)苯酚 (UV-327) 2,4-di-tert-butyl-6-(5-chlorobenzotriazol-2-yl)phenol (UV-327)	3864-99-1
166	2-(2H-benzotriazol-2-yl)-4-(tert-butyl)-6-(sec-butyl)phenol (UV-350) 2-(2H-苯并三唑-2-基)-4-三級丁基-6-二級丁基苯酚(UV-350)	36437-37-3
167	1,3-丙磺內酯 1,3-propanesultone	1120-71-4
168	全氟壬酸及其鈉與銨鹽 Perfluorononan-1-oic-acid and its sodium and ammonium salt	375-95-1 21049-39-8 4149-60-4
169	苯并(a)芘 Benzo[def]chrysene	50-32-8
170	雙酚 A 4,4’ -isopropylidenediphenol (bisphenol A)	80-05-7
171	4-庚基苯酚, 支鍊及直鍊 包括含有7 個碳烷基鏈的所有獨立的同分異構體和所有含有線性或分支7 個碳烷基鏈的UVCB 物質 '4-Heptylphenol, branched and linear [substances with a linear and/or branched alkyl chain with a carbon number of 7 covalently bound predominantly in position 4 to phenol, covering also UVCB- and well-defined substances which include any of the individual isomers or a combination thereof]	-
172	十九氟癸酸及其鈉和銨鹽 Nonadecafluorodecanoic acid (PFDA) and its sodium and ammonium salts	3108-42-7 335-76-2 3830-45-3
173	對(1,1-二甲基丙基)苯酚 p-(1,1-dimethylpropyl)phenol	80-46-6
174	全氟己基磺酸及其鹽類 Perfluorohexane-1-sulphonic acid and its salts (PFHxS)	355-46-4
175	1,2-苯并菲;(【艹快】) Chrysene	218-01-9
176	苯[a]蒽 Benz[a]anthracene	56-55-3
177	硝酸鎘 Cadmium nitrate	10325-94-7
178	氫氧化鎘 Cadmium hydroxide	21041-95-2

179	碳酸鎘 Cadmium carbonate	513-78-0
180	1,6,7,8,9,14,15,16,17,17,18, 18-十二氯五環 [12.2.1.16,9.02,13.05,10]十八碳-7,15-二烯(“Dechlorane Plus”TM)[含有其任何單獨的反式和順式異構體或其任何組合] 1,6,7,8,9,14,15,16,17,17,18,18-Dodecachloropentacyclo[12.2.1.16,9.02,13.05,10]octadeca-7,15-diene(“Dechlorane Plus”TM) [covering any of its individual anti- and syn-isomers or any combinationthereof]	-
181	1,3,4-噻二唑-2,5-二硫醇與甲醛和支鏈和直鏈4-庚基酚的反應產物(RP-HP) [含有≥0.1%w/w 支鏈和直鏈的4-庚基酚] Reaction products of 1,3,4-thiadiazolidine-2,5-dithione,formaldehyde and 4-heptylphenol, branched and linear (RP-HP) [with ≥0.1%w/w 4-heptylphenol, branched and linear]	-

Table 5-4. The 181 SVHC of the Regulation of Article 5 of (EC)

3.4 Product Composition

ISSI products are mainly dedicated to commercial / industrial / medical / mobile and automotive markets. Few selected ones are penetrating some advanced applications. To ensure that our products can comply with the regulations of environmental protection, ISSI has established a database that contains the information of product composition by package families. This database is confirmed with related assembly houses and its information is very important because it allows us to estimate the effectiveness of re-cycle and re-use rates of products and helps us answer customer’s End-Of-Life questions.

Table 5-5 below is an example sheet of material composition for thin small outline package (TSOP) family. The chemical characteristics are specified according to the components such as chip, gold wire or encapsulation. For each component, the material name, mass percentage, element, CAS[4] number and element weight are carefully calculated. Similar sheets are available for SOP, SOJ or other package families. Please contact us if you need more information.

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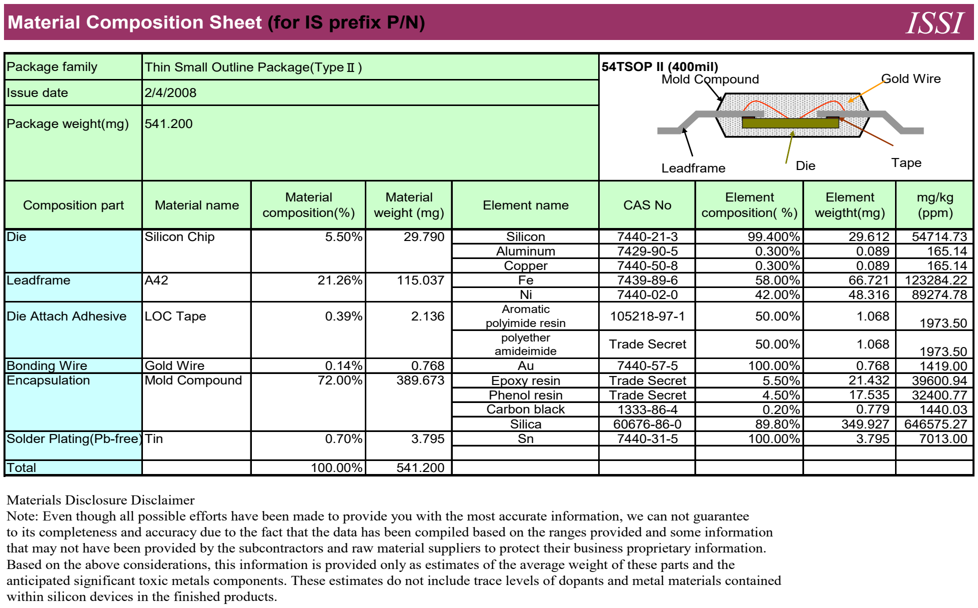
[4] CAS stands for Chemical Abstracts Service. It is a division of the American Chemical Society. Its registration number is widely used in MSDS (Materials Safety Data Sheet) to designate elements or compounds.



Material Composition Sheet (for IS prefix P/N) *ISSI*

Package family	Thin Small Outline Package(Type Ⅱ)	**54TSOP II (400mil)**
Issue date	2/4/2008	
Package weight(mg)	541.200	

Composition part	Material name	Material composition(%)	Material weight (mg)	Element name	CAS No	Element composition(%)	Element weigth(mg)	mg/kg (ppm)
Die	Silicon Chip	5.50%	29.790	Silicon	7440-21-3	99.400%	29.612	54714.73
				Aluminum	7429-90-5	0.300%	0.089	165.14
				Copper	7440-50-8	0.300%	0.089	165.14
Leadframe	A42	21.26%	115.037	Fe	7439-89-6	58.00%	66.721	123284.22
				Ni	7440-02-0	42.00%	48.316	89274.78
Die Attach Adhesive	LOC Tape	0.39%	2.136	Aromatic polyimide resin	105218-97-1	50.00%	1.068	1973.50
				polyether amideimide	Trade Secret	50.00%	1.068	1973.50
Bonding Wire	Gold Wire	0.14%	0.768	Au	7440-57-5	100.00%	0.768	1419.00
Encapsulation	Mold Compound	72.00%	389.673	Epoxy resin	Trade Secret	5.50%	21.432	39600.94
				Phenol resin	Trade Secret	4.50%	17.535	32400.77
				Carbon black	1333-86-4	0.20%	0.779	1440.03
				Silica	60676-86-0	89.80%	349.927	646575.27
Solder Plating(Pb-free)	Tin	0.70%	3.795	Sn	7440-31-5	100.00%	3.795	7013.00
Total		100.00%	541.200					

Materials Disclosure Disclaimer

Note: Even though all possible efforts have been made to provide you with the most accurate information, we can not guarantee to its completeness and accuracy due to the fact that the data has been compiled based on the ranges provided and some information that may not have been provided by the subcontractors and raw material suppliers to protect their business proprietary information. Based on the above considerations, this information is provided only as estimates of the average weight of these parts and the anticipated significant toxic metals components. These estimates do not include trace levels of dopants and metal materials contained within silicon devices in the finished products.

Table 5-5 Material Composition Sheet of 54 TSOP II

3.5 Lead-free Solution

3.5.1 Overview

Lead containing waste, disposed from PCB assembly, in landfills is eluded by acid rain, resulting in contaminated groundwater and rivers. When accumulated in the human body through drinking water or food, it will cause intellectual growth disorder in children.

The use of lead in electronic products is an important issue of global environmental protection. ISSI has received significant amount of requests regarding lead-free package demand from Japanese customers since early 2001. Consequently, ISSI has dedicated its resources to work with suppliers to provide lead-free solutions.

3.5.2 Background

For any alloy to be a worthwhile soldering material used in the electronic industry, it must possess certain specific qualities under the following criteria:

1) Melting Range:

It must have a liquids temperature that is sufficiently low so that components and boards are not damaged during soldering. In practice, this means that it must be usable at 260 degree C, which is the maximum temperature exposure limit for the majority of electronic components. Also, it must have a solidus temperature that is sufficiently high so that during service the solder joints do not lose their mechanical strength.[5]

2) Metallurgy:

Another crucial attribute of the alloy is that it must wet the common engineering metals and metallizations (silver, copper, nickel, etc). Ideally, new alloys should also be compatible with existing fluxes, stable and non-corrosive that they can withstand the stress/strain/temperature regimes encountered in electronic applications.

3) Environment Health and Safety Issues:

The alloy and its components must be non-toxic. Similar considerations apply to the soldering fluxes and the cleaning agents.

4) Economic and Supply Issues:

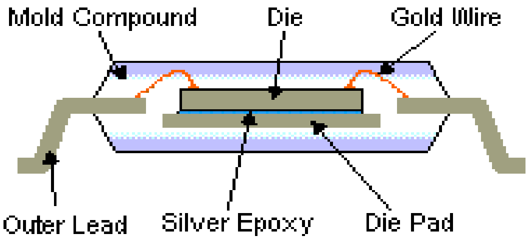
For any alloy to be considered as a potential replacement for tin-lead solder, its components must be in sufficient supply that it would not be subject to price constraints.

3.5.3 Lead-free Solder Solutions

There are a number of low melting point elements that can be combined to form feasible solder systems. The most practical solder systems are based on tin and bismuth or matte tin. ISSI has already provided millions of devices for memory products with lead-free external terminals. The composition and plating thickness of the lead-free solder solutions follow:

1) Outer lead:

⌖ Plating composition : Pure matte Tin Plating thickness: 300 to 800 micro-inches(7.6 to 20.3 um). The thickness of plating of curved region of shoulder and heel region due to the plating layer is stretched and will be reduce to min 3 um after lead forming.



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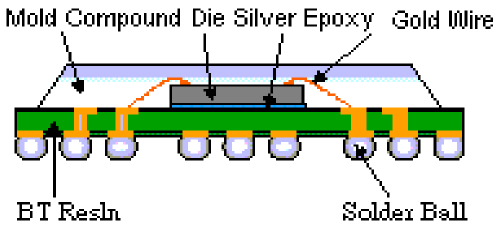
[5] The melting point of tin-lead eutectic at 183 °C provides a useful compromise between these two criteria.

2) Solder ball: Composition : 96.5 Sn 3.0 Ag 0.5 Cu

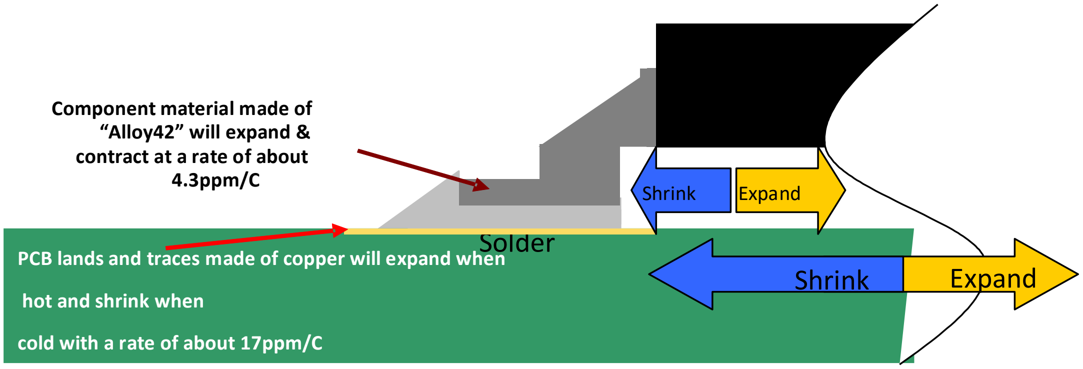


3) A copper lead frame with pure matte tin plating for SDRAM (optional).

ISSI is now offering an additional option for a range of DRAMs made of a copper lead frame with pure matte tin plating. The solution provides several reliability benefits, while reducing total cost of ownership.

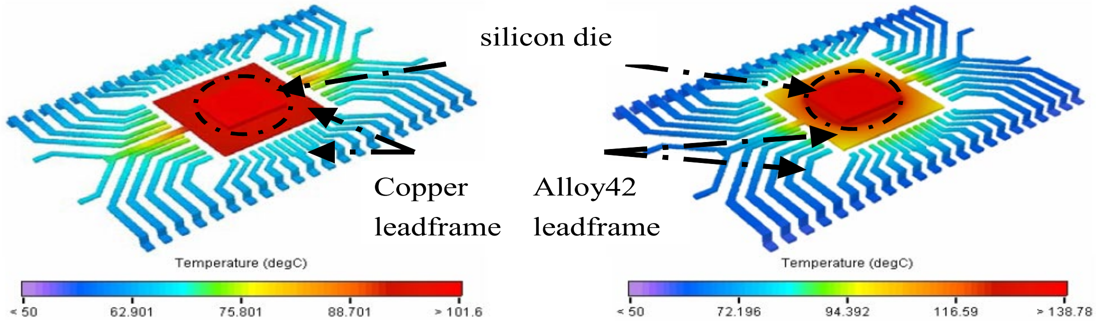
Better Joint Reliability

- The circuit boards in many applications will experience repeated temperature changes as time goes on.
- A problem can arise because every kind of material on the surface of the board has a different responsiveness to heat, often referred to as its coefficient of thermal expansion (CTE).
- Eventually, solder joints can crack from the pulling forces of expansion and contraction. When a part with a conventional Alloy42 lead frame is mounted on a copper surface, there would be approximately a 3-to-1 ratio of expansion /contraction.
- Parts made with a copper lead frame expand and contract the same amount as the copper pads, minimizing the stresses at the joints.

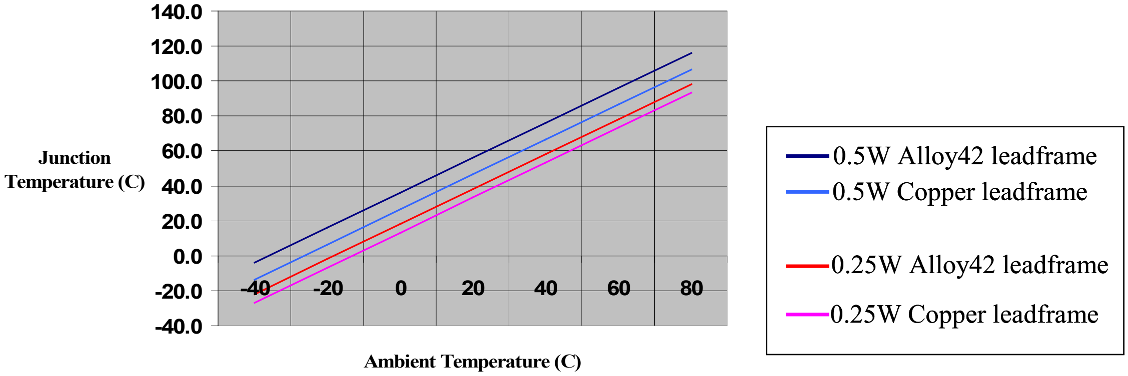


Better Thermal Dissipation

- A hypothetical analysis was made of two components that are identical, except for their leadframe materials. Both have the same power draw (1 watt), and sit in the same ambient air temperature (50°C).



- Mostly due to the lesser thermal conductance of the Alloy42 metal, the chip on the right reaches a temperature of about 139°C, but the chip on the left sits at a relatively cooler 102°C.with typical power use, the chip in the copper leadframe package would be about 5°C to 10°C cooler than the one in the Alloy42 package.



3.6 Halogen-free Solution

3.6.1 Overview

In epoxy molding compounds and substrates, halogens and antimony trioxide are usually used as flame retardant to meet UL94V-0 requirement. When electronic products contain those substances are disposed and incinerated, it is possible to produce harmful dioxins.

3.6.2 Halogen-free Compound Status

When normal compounds are replaced with phosphorous and inorganic compounds, the moldability and reliability may be lessened. However, several industrial consortia and ISSI assemblers have evaluated halogen-free compound. Safe materials for replacement have been successfully developed with wide molding window and excellent reliability, and are commercially available now. The providers include Hitachi Chemical, Sumitomo Bakelite, ShinEtsu, Kyocera etc… ISSI is currently ready to provide samples or components with halogen-free[6] compound for lead-free packages upon customer's request.

3.6.3 Halogen-free Substrate Status

Several industry consortia and ISSI assemblers have also evaluated halogen-free substrate. Safe materials for replacement have been successfully developed and are commercially available now. ISSI is currently ready to provide samples with halogen-free substrate for lead-free packages[7] upon customer's request.

3.7 Pb-free/Halogen-free Evaluation/Qualification Information

3.7.1 Commercial / Industrial Grade Products

The evaluation/qualification of products for general purpose is carried out in two stages. One is the standard procedure that includes preconditioning test and environmental tests. The other is the evaluation/qualification of solder plating.

1) Component or Package Level Tests
In this stage, the qualification items and procedures are similar to that of the regular packages as described in chapter 3. The details are shown in Table 5-6 and the major difference is that the IR reflow temperature of preconditioning is higher (260 °C).

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[6] Halogen-free will cause further cost increment in comparison with lead-free. Material supply chain availability and cost concern in new material will rely on market demand in green product.

[7] The suitable halogen-free substrate for lead-free package will be available after meeting criteria specified in JEDEC level 3 with triple IR reflows @ 260 degree C.

Reliability Test Items	Test Method	Test Conditions	S/S	Acc/Rej
Preconditioning MSL 3 (Heat resistance test included)	JESD22-A113 & J-STD-020	30C / 60%RH / 192hrs + 260C IR x 3	240	0/1
TCT (Temp cycling)	JESD22-A104	- 65 to 150 C / 500 cycles	77	0/1
PCT (Autoclave or pressure cooker)	JESD22-A102	121 C / 100 %RH / 15 psi / 168 hrs (Not apply for BGA packages)	77	0/1
HAST (Highly Accelerated Stress Test)	JESD22-A110	130C / 85%RH / 33.3 psi / 96 hrs	77	0/1

Table 5-6 Component level tests

2) Solder Plating Quality/Reliability Evaluation

The solder paste and solder plating material used in Pb-free package require higher temperature in the SMT process because these materials have higher melting point. To ensure the transition from regular package to Pb-free package will not result in detrimental failure, it is crucial to examine the mechanical properties of the solder joints, which determines the resistance to installation and handling mechanics.

Before the solder joint test, the package will go through the SMT process in which the preheating temperature is ramping up from 130 °C to 170 °C within 45 to 90 seconds. Then the package is heated to 225 °C or more within 20 to 30 seconds. The peak temperature is 230 °C or less at solder joint of terminal. The solder paste is Sn/3.0 Ag/0.5 Cu.

Solder joint strength tests are carried out by two items:

Item 1: lead pull strength

- all the packages will go through the pretreatment of moisture soaking at 105 °C under 100% relative humidity for 4 hours
- perform TCT test under the condition of –35 °C to 85°C with 30 minutes/cycle
- measure lead pull strength at 0, 250, 500 and 1000 cycles.

The pass criterion requires that the final lead pull strength has to exceed half of the initial values.

Item 2: cross-sectional view study

- perform SEM cross-sectional view study after 0, 250, 500 and 1000 cycles.

The pass criterion requires that the final solder joint width has to exceed half of the initial values.

3.7.2 Advanced Electronic Grade Products

For products used in advanced applications, we will either introduce extra test items or tighten the test conditions/criteria.

1) Component or Package Level Tests
For component level test, we add HTSL (High Temperature Storage Life) item to check the resistance of package to the prolonged high temperature storage condition.

For stricter test conditions/criteria, first of all, all the acceptance criteria allow zero failures only. In addition, final test (FT) check before and after the test is a must for all the test items involved. In some cases, FT at various temperatures are also specified such as in the PCT and HTSL tests as shown in Table 5-7.

Reliability Test Items	**Reference Doc.**	**Test Method**	**Sample size/Lot**	**Accept Criteria**	**Notes**
Preconditioning (Heat resistance test included)	AEC-Q100#A1	J-STD-020 & JESD22A113	231/ 3 lots	0 fails	MSL3 at least. PC performed prior to TCT, PCT and THB/HAST stresses. F/T checked before and after at room temp. Delamination from die surface is acceptable if the device can pass subsequent qualification tests.
TCT (Temperature Cycling)	AEC-Q100#A4	JESD22A104	77/ 3 lots	0 fails	Grade 1 : -65C~150C, 500 cycles. F/T checked before and after at high temp. Decap procedure on 5 units/ 1 lot after test completed, and perform wire pull test on 2 corner bonds per corner and 1 mid-bond per side.
PCT (Autoclave or Pressure cooker)	AEC-Q100#A3	JESD22A102 or A118	77/ 3 lots	0 fails	121C/15psi/168 hrs (Not apply for BGA packages). F/T checked before and after at room temp.
THB (Temp Humidity Bias) or HAST (Highly Accelerated Stress Test)	AEC-Q100#A2	JESD22A101 or A110	77/ 3 lots	0 fails	THB: 85C/85%RH/1000 hrs with bias or HAST: 130C/85%RH/33.3psi/96 hrs or 110C/85%RH/17.7psi/264hrs with bias. F/T checked before and after at room and high temp.

HTSL (High Temp Storage Life)	AEC-Q100#A6	JESD22A103	45/ 1 lot	0 fails	Grade 1 : 150C, 1000 hrs. F/T checked before and after at room and high temp.

Table 5-7 Component level tests for advanced applications

2) Solder Plating Quality/Reliability Evaluation

Besides the aforementioned solder joint strength test, three more test items are added for advanced electronic applications. They are: the solderability and wettability test, the tin whisker check, and the electrical continuity check with Daisy Chain.

a) Solderability and wettability test

This test determines the solderability of terminals after transportation and storage. Equilibrium method will be adopted to measure the Meniscus force curve. The acceptance criterion requires the zero cross time to be less than 3 seconds.

b) Tin whisker

The extent of tin whisker growth of Pb-free package is much worse than in the regular package because the built-in stress is quite different. If this reliability issue is not well taken care of, the product might get shorted after prolonged service in the field.

The tin whisker tests will be carried out with three different approaches:

- perform TCT test under the condition of –55 °C to 85 °C with 10 minutes soak ; 3 cycles / hour for 1500 cycles .
- perform THT (Temperature humidity storage) under the condition of 30 ± 2 °C and 60 ±3% RH relative humidity for 4,000 hrs.
- perform THT (High temperature humidity storage) under the condition of 55 ± 3 °C and 85 ±3 % RH relative humidity for 4,000 hrs.

After the tests, the length of any tin whisker will be checked. The acceptance criterion is 45 μm maximum for TCT testing & 40 um for temperature humidity storage (Room Temp & High Temp) by stereoscope at 40X or SEM at 300X above.
ISSI implements annealing process to reduce tin whisker growth, for the pure matte tin of terminal is performed the heat treatment with 1hr @ 150 ℃ within 24 hrs after plating process.

c) Daisy chain

For this test, we will perform preconditioning test and TCT test for 3000 cycles. The acceptance criterion is that the electrical continuity should be guaranteed after 3000 cycles.

3.8 Current Status

The development work on lead-free solders has been launched by a number of organizations and institutions through either formal partnership or professional alliance in U.S., Europe and Japan. The qualified lead-free and halogen-free packages for mass production.

However, both lead-containing and lead-free packages will be provided in parallel for customers' choice.

3.9 Solder Heat Resistance for PCBA (PC Board Assembly)

Surface Mount devices (SMD) have become popular in recent years due to their advantage in high-density mounting. However, SMD package delamination often occurring between the chip/die pad and the molding compound, caused by thermal stress during mounting, has also become a problem. To assure all ISSI's products not plagued by this problem, all lead-free packages are required to meet JEDEC standard, Level 3. The recommended soldering methods and constraints are described below:

1) Reflow soldering method

Peak temperature: 260 ℃ maximum, 30 seconds, soldering zone: 217 ℃ or more, 60 to 150 seconds, number of cycles: 3 cycles

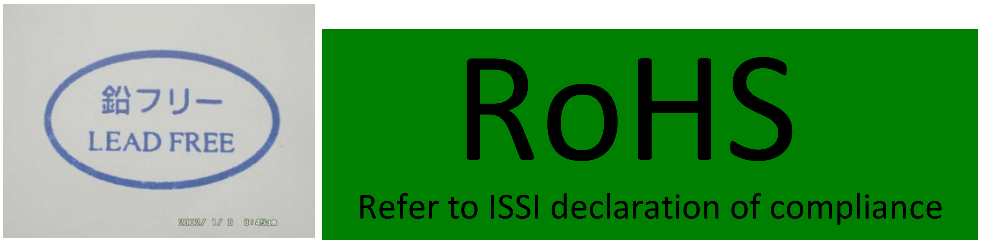
2) Soldering iron method:
Temperature: 380 ℃ max., application time of soldering iron: 5 seconds maximum, number of cycles: 2 cycles

3.10 Lead Time from Ordering to Delivery

The maximum lead-time from ordering to delivery, for sample evaluation and mass production on unqualified lead-free and halogen-free products, is 2 and 3.5 months respectively. Should you have any comments, suggestions, or questions, please contact ISSI regional Sales office for details.

3.11 Distinguishing Mark of Lead-free and RoHS compliance Package

1) **Add an "L" or a “G” to the end of the part number. Please refer to the documents of packing and IC top mark.**
2) Add lead-free discrimination stamp on dry pack, inner box and outer box (Fig. 5-3a)
3) Add RoHS label on reel, dry pack, inner box and outer box (Fig. 5-3b).



(b)

Figure 5-3 Discrimination stamp & RoHS Label

3.12 Re-flow Temperature Profile for Lead-free Package

Pb-free Process – Package Classification Reflow Temperatures

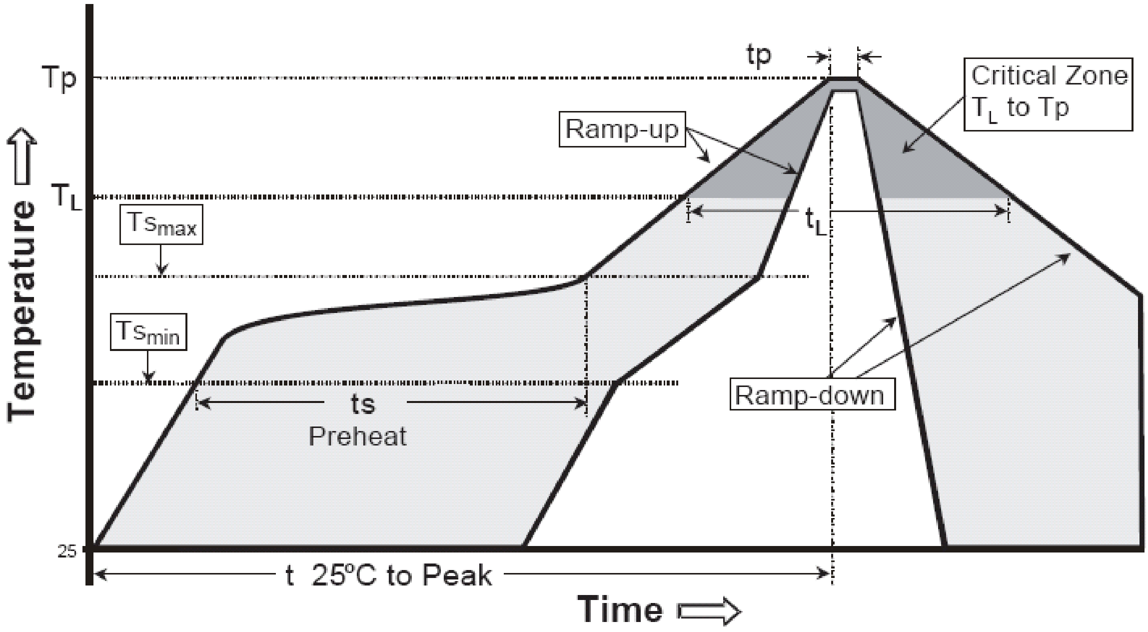
Package Thickness	Volume mm^3<350	Volume mm^3: 350- 2000	Volume mm^3>2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Profile Feature	Pb-free Assembly
Ramp-Up Rate(TL to Tp)	3 °C/second max.
Preheat– Temperature Min (Tsmin) to Max (Tsmax)	150~200 °C
– Time (tsmin to tsmax)	60-120 seconds
Time maintained above – Temperature (TL)	217 °C
– Time (tL)	60-150 seconds
Peak Temperature (Tp) (Note 2)	See package classification
Time within 5 °C of actual Peak,Temperature (tp)	30 seconds (Note 3)
Ramp-Down Rate(Tp to TL)	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.
Number of applicable Temperature cycles	3 cycles max.

Notes: 1. All temperatures refer to top side of the package, measured on the package body surface.

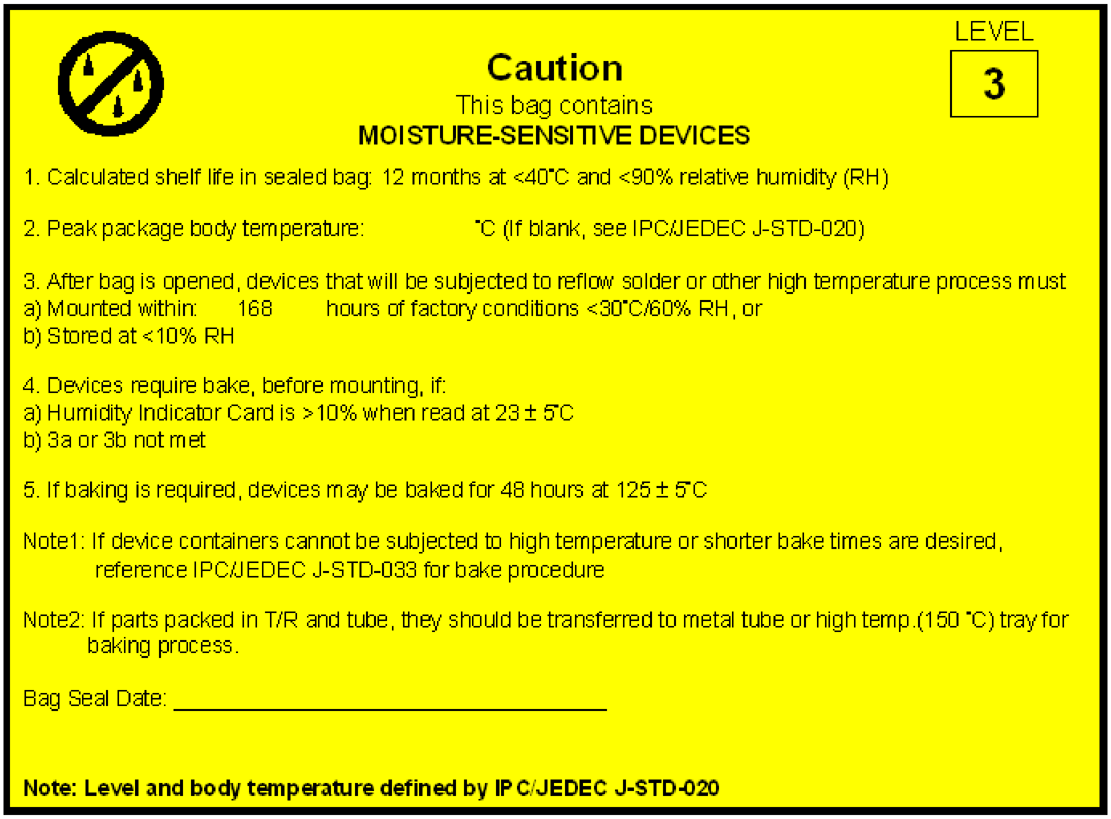
2. The peak temperature (Tp) is defined as package heatproof min. and customer used max.

3. The time at peak temperature (tp) is defined as package heatproof min. and customer used max.



Storage Recommendations

5.3.13 Recommended Storage Condition



LEVEL

3

Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

1. Calculated shelf life in sealed bag: 12 months at <40˚C and <90% relative humidity (RH)

2. Peak package body temperature: ˚C (If blank, see IPC/JEDEC J-STD-020)

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
a) Mounted within: 168 hours of factory conditions <30˚C/60% RH, or
b) Stored at <10% RH

4. Devices require bake, before mounting, if:
a) Humidity Indicator Card is >10% when read at 23 ± 5˚C
b) 3a or 3b not met

5. If baking is required, devices may be baked for 48 hours at 125 ± 5˚C

Note1: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Note2: If parts packed in T/R and tube, they should be transferred to metal tube or high temp.(150 ˚C) tray for baking process.

Bag Seal Date: ______________________________

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

3.14 ISSI Declaration of Compliance

ISSI issues a letter of declaration to certify that parts are compliant to:

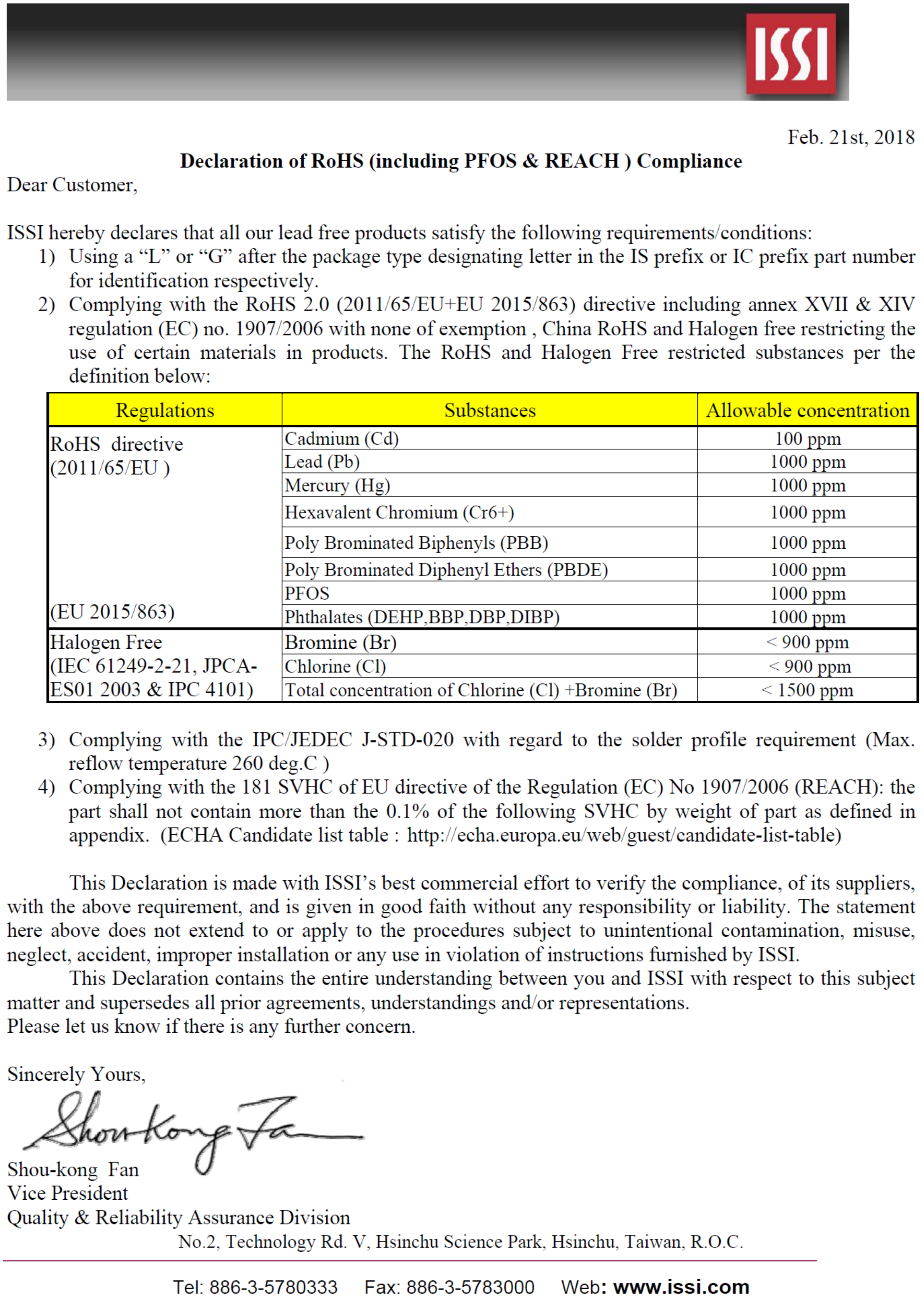
1) RoHS (EU Directive entitled “Restriction on the use of certain Hazardous Substances 2011/65/EU, and 2006/122/EC”) requirements and containing none of the following 7 substances: Pb, Hg, Cd, Cr(VI), PBB, PBDE, and PFOS.

2) The 181 SVHC (Substance of Very High concern) of EU directive of the Regulation (EC) No 1907/2006 (REACH): the part shall not contain more than the 0.1% of the following SVHC by weight of part as defined in appendix also including annex XVII.

3) IEC 61249-2-21, JPCA-ES01 2003 & IPC 4101, the Br, Cl , must be lower than 900 ppm, respectively, and total amount of PPM must be lower than 1500 ppm (Br + Cl < 1500 ppm).

4) Conflict Materials and EICC by not using the materials from mines with inferior working conditions, such as DRC (Democratic Republic of the Congo). The suppliers or subcontractors will trace the supply chain for gold (Au), tantalum (Ta), tungsten (W), tin (Sn) and cobalt (Co).

RoHS Declaration



Feb. 21st, 2018

Declaration of RoHS (including PFOS & REACH) Compliance

Dear Customer,

ISSI hereby declares that all our lead free products satisfy the following requirements/conditions:

1) Using a "L" or "G" after the package type designating letter in the IS prefix or IC prefix part number for identification respectively.
2) Complying with the RoHS 2.0 (2011/65/EU+EU 2015/863) directive including annex XVII & XIV regulation (EC) no. 1907/2006 with none of exemption , China RoHS and Halogen free restricting the use of certain materials in products. The RoHS and Halogen Free restricted substances per the definition below:

Regulations	Substances	Allowable concentration
RoHS directive (2011/65/EU)	Cadmium (Cd)	100 ppm
	Lead (Pb)	1000 ppm
	Mercury (Hg)	1000 ppm
	Hexavalent Chromium (Cr6+)	1000 ppm
	Poly Brominated Biphenyls (PBB)	1000 ppm
	Poly Brominated Diphenyl Ethers (PBDE)	1000 ppm
	PFOS	1000 ppm
(EU 2015/863)	Phthalates (DEHP,BBP,DBP,DIBP)	1000 ppm
Halogen Free (IEC 61249-2-21, JPCA-ES01 2003 & IPC 4101)	Bromine (Br)	< 900 ppm
	Chlorine (Cl)	< 900 ppm
	Total concentration of Chlorine (Cl) +Bromine (Br)	< 1500 ppm

3) Complying with the IPC/JEDEC J-STD-020 with regard to the solder profile requirement (Max. reflow temperature 260 deg.C)
4) Complying with the 181 SVHC of EU directive of the Regulation (EC) No 1907/2006 (REACH): the part shall not contain more than the 0.1% of the following SVHC by weight of part as defined in appendix. (ECHA Candidate list table : http://echa.europa.eu/web/guest/candidate-list-table)

This Declaration is made with ISSI's best commercial effort to verify the compliance, of its suppliers, with the above requirement, and is given in good faith without any responsibility or liability. The statement here above does not extend to or apply to the procedures subject to unintentional contamination, misuse, neglect, accident, improper installation or any use in violation of instructions furnished by ISSI.

This Declaration contains the entire understanding between you and ISSI with respect to this subject matter and supersedes all prior agreements, understandings and/or representations.

Please let us know if there is any further concern.

Sincerely Yours,

Shou Kong Fa

Shou-kong Fan
Vice President
Quality & Reliability Assurance Division

No.2, Technology Rd. V, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.

Tel: 886-3-5780333 Fax: 886-3-5783000 Web: **www.issi.com**

Appendix: Complying with 181 SVHC (substance of very high concern) of the Regulation (EC) No 1907/2006 (REACH)

Revision: Jan. 2018

No.	Substance Name	CAS No.
1	三乙基砷酸酯 Triethyl arsenate	15606-95-8
2	蒽 Anthracene	120-12-7
3	4,4'- 二氨基二苯甲烷 4,4'- Diaminodiphenylmethane(MDA)	101-77-9
4	鄰苯二甲酸二丁酯 Dibutyl phthalate(DBP)	84-74-2
5	氯化鈷 Cobalt dichloride	7646-79-9
6	五氧化二砷 Diarsenic Pentaoxide	1303-28-2
7	三氧化二砷 Diarsenic trioxide	1327-53-3
8	重鉻酸鈉，二倍結晶水 Sodium Dichromate	7789-12-0 10588-01-9
9	5-叔丁基-2,4,6-三硝基間二甲苯 5-tert-butyl-2,4,6-trinitro-m-xylene(musk xylene)	81-15-2
10	鄰苯二甲酸二(2-乙基已基)酯 Bis(2-ethylhexyl) Phthalate (DEHP)	117-81-7
11	六溴環十二烷 Hexabromocyclododecane (HBCDD) and all major diastereoisomers identified: Alpha-hexabromocyclododecane Beta-hexabromocyclododecane Gamma-hexabromocyclododecane	25637-99-4 3194-55-6 134237-50-6 134237-51-7 134237-52-8
12	短鏈氯化路蠟 Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins)	85535-84-8
13	氧化三丁錫 Bis(tributyltin)oxide (TBTO)	56-35-9
14	砷酸氫鉛 Lead hydrogen arsenate	7784-40-9
15	鄰苯二甲酸丁酯苯甲酯 Benzyl butyl phthalate (BBP)	85-68-7
16	蒽油 Anthracene oil	90640-80-5
17	蒽油，蒽糊，輕油 Anthracene oil, anthracene paste, distn. Lights*	91995-17-4
18	蒽油，蒽糊，蒽餾分離液 Anthracene oil, anthracene paste, anthracene fraction	91995-15-2
19	蒽油，含蒽量少 Anthracene oil, anthracene-low	90640-82-7
20	蒽油，蒽糊 Anthracene oil, anthracene paste	90640-81-6
21	煤瀝青，高溫 Coal tar pitch, high tempperature	65996-93-2
22	丙烯醯胺 Acrylamide	79-06-1
23	矽酸鋁，陶瓷耐火纖維 Aluminosilicate Refractory Ceramic Fibres are fibres covered by index number 650-017-00-8 in Annex VI, part 3, table 3.1 of Regulation (EC) No 1272/2008 of the European Parliament and of the Council of 16 December 2008 on classification, labelling and packaging of substances and mixtures, and fulfil the three following conditions: a) oxides of aluminium and silicon are the main components present (in the fibres) within variable concentration ranges b) fibres have a length weighted geometric mean diameter less two standard geometric errors of 6 or less micrometres (μm) c) alkaline oxide and alkali earth oxide (Na2O+K2O+CaO+MgO+BaO) content less or equal to 18% by weight	None

24	矽酸鋁氧化鋯，陶瓷耐火纖維 Zirconia Aluminosilicate, Refractor Ceramic Fibres are fibres covered by index number 650-017-00-8 in Annex VI, part 3, table 3.1 of Regulation (EC) No 1272/2008 of the European Parliament and of the Council of 16 December 2008 on classification, labelling and packaging of substances and mixtures, and fulfil the three following conditions: a) oxides of aluminium, silicon and zirconium are the main components present (in the fibres) within variable concentration ranges b) fibres have a length weighted geometric mean diameter less two standard geometric errors of 6 or less micrometres (µm). c) alkaline oxide and alkali earth oxide (Na2O+K2O+CaO+MgO+BaO) content less or equal to 18% by weight	None
25	2,4 二硝基甲苯 2,4-Dinitrotoluene	121-14-2
26	鄰苯二甲酸二異丁酯 DiIsobutyl phthalate	84-69-5
27	鉻酸鉛 Lead chromate	7758-97-6
28	紅色鉬鉻酸硫酸鹽 Lead chromate molybdate sulphate red (C.I. Pigment Red 104)	12656-85-8
29	黃色硫化鉻酸鉛 Lead sulfochromate yellow (C.I. Pigment Yellow 34)	1344-37-2
30	三 2-(氯乙基)磷酸酯 Tris (2-chloroethyl) phosphate	115-96-8
31	三氯乙烯 Trichloroethylene	79-01-6
32	硼酸 Boric acid	10043-35-3 11113-50-1
33	無水四硼酸二鈉 Disodium tetraborate, anhydrous	1303-96-4 1330-43-4 12179-04-3
34	水合七氧四硼酸二鈉 Tetraboron disodium heptaoxide, hydrate	12267-73-1
35	鉻酸鈉 Sodium chromate	7775-11-3
36	鉻酸鉀 Potassium chromate	7789-00-6
37	重鉻酸銨 Ammonium dichromate	7789-09-5
38	重鉻酸 Potassium dichromate	7778-50-9
39	硫酸鈷 Cobalt sulfate	10124-43-3
40	硝酸鈷 Cobalt dinitrate	10141-05-6
41	碳酸鈷 Cobalt carbonate	513-79-1
42	醋酸鈷 Cobalt diacetate	71-48-7
43	2-甲氧基乙醇 2-Methoxyethanol	109-86-4
44	2-乙氧基乙醇 2-Ethoxyethanol	110-80-5
45	三氧化鉻 Chromium trioxide	1333-82-0
46	三氧化二鉻 Chromic acid/重鉻酸 Dichromic acid	7738-94-5 13530-68-2
47	乙酸-2-乙氧基乙酯 2-ethoxyethyl acetate	111-15-9
48	鉻酸鍶 Strontium chromate	7789-06-2
49	鄰苯二甲酸二(C7-11 支鏈與直鏈)烷基酯 1,2-Benzenedicarboxylic acid, di-C7-11-branched and linear alkyl esters (DHNUP)	68515-42-4
50	肼 Hydrazine	302-01-2 7803-57-8
51	N-甲基吡咯烷酮 1-methyl-2-pyrrolidone	872-50-4
52	1，2，3-三氯丙烷 1,2,3-trichloropropane	96-18-4
53	鄰苯二甲酸二 C6-8 支链 烷基酯 1,2-Benzenedicarboxylic acid, di-C6-8-branched alkyl esters, C7-rich (DIHP)	71888-89-6

54	鉻酸鉻 Dichromium tris(chromate)	24613-89-6
55	氫氧化鉻酸鋅鉀 Potassium hydroxyoctaoxodizincatedi-chromate	11103-86-9
56	C.I.顏料黃 36 Pentazinc chromate octahydroxide	49663-84-5
57	甲醛和苯胺聚合物 Formaldehyde, oligomeric reaction products with aniline (technical MDA)	25214-70-4
58	鄰苯二甲酸二甲氧乙酯 Bis(2-methoxyethyl) phthalate	117-82-8
59	鄰-甲氧苯胺 2-Methoxyaniline; o-Anisidine	90-04-0
60	4-三級辛基苯酚 4-(1,1,3,3-tetramethylbutyl)phenol, (4-tert-Octylphenol)	140-66-9
61	1,2-二氯乙烷 1,2-Dichloroethane	107-06-2
62	二甘醇二甲醚 Bis(2-methoxyethyl) ether	111-96-6
63	砷酸 Arsenic acid	7778-39-4
64	砷酸鈣 Calcium arsenate	7778-44-1
65	砷酸鉛 Trilead diarsenate	3687-31-8
66	N,N-二甲基乙醯胺 N,N-dimethylacetamide (DMAC)	127-19-5
67	4,4'-二氨基-2,2'-二氯二苯甲烷， 2,2'-dichloro-4,4'-methylenedianiline (MOCA)	101-14-4
68	酚酞 Phenolphthalein	77-09-8
69	疊氮化鉛 Lead azide Lead diazide	13424-46-9
70	收斂酸鉛 Lead styphnate	15245-44-0
71	苦味酸鉛 Lead dipicrate	6477-64-1
72	三甘醇二甲醚 1,2-bis(2-methoxyethoxy)ethane (TEGDME; triglyme)	112-49-2
73	乙二醇二甲醚 1,2-dimethoxyethane; ethylene glycol dimethyl ether (EGDME)	110-71-4
74	α,α-二[(二甲氨基)苯基]-4-甲氨基苯甲醇 4,4'-bis(dimethylamino)-4''-(methylamino)trityl alcohol	561-41-1
75	4'-二(N,N-二甲氨基)二苯甲酮 4,4'-bis(dimethylamino)benzophenone (Michler's ketone)	90-94-8
76	结晶紫 [4-[4,4'-bis(dimethylamino) benzhydrylidene]cyclohexa-2,5-dien-1-ylidene]dimethylammonium chloride (C.I. Basic Violet 3)	548-62-9
77	碱性蓝 26; 维多利亞藍 B [4-[[4-anilino-1-naphthyl][4-(dimethylamino)phenyl]methylene]cyclohexa-2,5-dien-1-ylidene] dimethylammonium chloride (C.I. Basic Blue 26)	2580-56-5
78	三氧化二硼 (無水硼酸) Diboron trioxide	1303-86-2
79	氨基甲醛 Formamide	75-12-7
80	甲基磺酸铅 Lead(II) bis(methanesulfonate)	17570-76-2
81	N,N,N'N'-四甲基-4,4'-二氨基二苯甲烷 N,N,N',N'-tetramethyl-4,4'-methylenedianiline (Michler's base)	101-61-1
82	1,3,5-三缩水甘油-S-三嗪三酮 TGIC (1,3,5-tris(oxiranylmethyl)-1,3,5-triazine-2,4,6(1H,3H,5H)-trione)	2451-62-9
83	A,A-二[4-(二甲氨基)苯基]-4-苯基氨基-1-萘甲醇 α,α-Bis[4-(dimethylamino)phenyl]-4 (phenylamino)naphthalene-1-methanol (C.I. Solvent Blue 4)	6786-83-0
84	β-TGIC (1,3,5-tris[(2S and 2R)-2,3-epoxypropyl]-1,3,5-triazine-2,4,6-(1H,3H,5H)-trione) 异氰脲酸 B-三缩水甘油酯	59653-74-6
85	十溴聯苯醚 Bis(pentabromophenyl) ether (DecaBDE)	1163-19-5
86	全氟十三酸 Pentacosafluorotridecanoic acid	72629-94-8
87	全氟十二烷酸 Tricosafluorododecanoic acid	307-55-1
88	全氟十一烷酸 Henicosafluoroundecanoic acid	2058-94-8
89	全氟代十四酸 Heptacosafluorotetradecanoic acid	376-06-7

120	四乙基鉛 Tetraethyllead	78-00-2
121	三鹹式硫酸鉛 Tetralead trioxide sulphate	12202-17-4
122	磷酸氧化鉛 Trilead dioxide phosphonate	12141-20-7
123	呋喃 Furan	110-00-9
124	環氧丙烷 Propylene oxide; 1,2-epoxypropane; methyloxirane	75-56-9
125	硫酸二乙酯 Diethyl sulphate	64-67-5
126	硫酸二甲酯 Dimethyl sulphate	77-78-1
127	3-乙基-2-甲基-2-(3-甲基丁基)噁唑烷 3-ethyl-2-methyl-2-(3-methylbutyl)-1,3-oxazolidine	143860-04-2
128	地樂酚 Dinoseb	88-85-7
129	4,4'-二氨基-3,3'-二甲基二苯甲烷 4,4'-methylenedi-o-toluidine	838-88-0
130	4,4'-二氨基二苯醚 4,4'-oxydianiline and its salts	101-80-4
131	4-胺基偶氮苯 4-Aminoazobenzene; 4-Phenylazoaniline	60-09-3
132	2,4-二氨基甲苯 4-methyl-m-phenylenediamine (2,4-toluene-diamine)	95-80-7
133	6-甲氧基 -間-甲苯胺 甲苯胺 6-methoxy-m-toluidine (p-cresidine)	120-71-8
134	4-氨基聯苯 Biphenyl-4-ylamine	92-67-1
135	鄰氨基偶氮甲苯 o-aminoazotoluene	97-56-3
136	鄰甲基苯胺 o-Toluidine; 2-Aminotoluene	95-53-4
137	N-甲基乙酰胺 N-methylacetamide	79-16-3
138	溴代正丙烷 1-bromopropane; n-propyl bromide	106-94-5
139	鎘 Cadmium	7440-43-9
140	氧化鎘 Cadmium oxide	1306-19-0
141	鄰苯二甲酸二戊酯 Dipentyl phthalate (DPP)	131-18-0
142	分支或線性的乙氧化壬基酚，包括含有 9 個碳烷基鏈的所有獨立的同分異構體和所有含有線性或分支 9 個碳烷基鏈的 UVCB 物質 4-Nonylphenol, branched and linear, ethoxylated [substances with a linear and/or branched alkyl chain with a carbon number of 9 covalently bound in position 4 to phenol, ethoxylated covering UVCB- and well-defined substances, polymers and homologues, which include any of the individual isomers and/or combinations thereof]	-
143	全氟辛酸銨 Ammonium pentadecafluorooctanoate (APFO)	3825-26-1
144	全氟辛酸 Pentadecafluorooctanoic acid (PFOA)	335-67-1
145	硫化鎘 Cadmium sulphide	1306-23-6
146	鄰苯二甲酸二己酯 Dihexyl phthalate	84-75-3
147	直接紅 28 Disodium 3,3'-[[1,1'-biphenyl]-4,4'-diylbis(azo)]bis(4-aminonaphthalene-1-sulphonate) (C.I. Direct Red 28)	573-58-0
148	直接黑 38 Disodium 4-amino-3-[[4'-[(2,4-diaminophenyl)azo][1,1'-biphenyl]-4-yl]azo] -5-hydroxy-6-(phenylazo)naphthalene-2,7-disulphonate (C.I. Direct Black 38)	1937-37-7
149	亞乙基硫脲 Imidazolidine-2-thione; 2-imidazoline-2-thiol	96-45-7
150	醋酸鉛 Lead di (acetate)	301-04-2
151	磷酸三（二甲苯）酯 Trixylyl phosphate	25155-23-1
152	鄰苯二甲酸二己酯（支鏈和直鏈）1,2-Benzenedicarboxylic acid, dihexyl ester,branched and linear	68515-50-4

153	氯化鎘 Cadmium chloride	10108-64-2
154	過硼酸鈉 Sodium perborate; perboric acid, sodium salt	15120-21-5
155	過氧偏硼酸鈉 Sodium peroxometaborate	7632-04-4
156	2-(2’ -羥基-3’ ,5’ -二-叔-戊基苯基)苯並三唑 (紫外線吸收劑 328) 2-(2H-benzotriazol-2-yl)-4,6-ditertpentylphenol (UV-328)	25973-55-1
157	2-[2-羥基-3’ ,5’ -二-叔-丁基苯基]-苯並三唑 (紫外線吸收劑 320) 2-benzotriazol-2-yl-4,6-di-tert-butylphenol (UV-320)	3846-71-7
158	二正辛基-双（2-乙基己基巰基乙酸酯）錫 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (DOTE)	15571-58-1
159	氟化镉 Cadmium fluoride	7790-79-6
160	硫酸鎘 Cadmium sulphate	10124-36-4; 31119-53-6
161	二正辛基-双（2-乙基己基巰基乙酸酯）錫和單辛基-三(2-乙基己基巰基乙酸酯）錫的反應物 Reaction mass of 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate and 2-ethylhexyl 10-ethyl-4-[[2-[(2-ethylhexyl)oxy]-2-oxoethyl]thio]-4-octyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (reaction mass of DOTE and MOTE)	-
162	鄰苯二甲酸二(C6-C6)烷基酯：(癸基，己基，辛基)酯與 1，2-鄰苯二甲酸的複合物且鄰苯二甲酸二己酯含量≥ 0.3% 1,2-benzenedicarboxylic acid, di-C6-10-alkyl esters; 1,2-benzenedicarboxylic acid, mixed decyl and hexyl and octyl diesters with ≥ 0.3% of dihexyl phthalate (EC No. 201-559-5)	68515-51-5 68648-93-1
163	5-仲丁基-2-（2,4-二甲基環丁-3-烯-1-基）-5-甲基-1,3-二惡烷[1]，5-仲丁基-2-（4,6-二甲基環己-3-烯-1-基）-5-甲基-1,3-二惡烷[2] [覆蓋任何[1]和[2]或者其任意組合的單獨的異構體 (卡拉花醛及其同分易構物) 5-sec-butyl-2-(2,4-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [1], 5-sec-butyl-2-(4,6-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [2] [covering any of the individual stereoisomers of [1] and [2] or any combination thereof]	-
164	硝苯 Nitrobenzene	98-95-3
165	2,4-貳三級丁基-6-(5-氯苯三唑-2-基)苯酚 (UV-327) 2,4-di-tert-butyl-6-(5-chlorobenzotriazol-2-yl)phenol (UV-327)	3864-99-1
166	2-(2H-benzotriazol-2-yl)-4-(tert-butyl)-6-(sec-butyl)phenol (UV-350) 2-(2H-苯并三唑-2-基)-4-三級丁基-6-二級丁基苯酚(UV-350)	36437-37-3
167	1,3-丙磺內酯 1,3-propanesultone	1120-71-4
168	全氟壬酸及其鈉與銨鹽 Perfluorononan-1-oic-acid and its sodium and ammonium salt	375-95-1 21049-39-8 4149-60-4

169	苯并(a)芘 Benzo[def]chrysene	50-32-8
170	雙酚 A 4,4’ -isopropylidenediphenol (bisphenol A)	80-05-7
171	4-庚基苯酚, 支鍊及直鍊　包括含有 7 個碳烷基鏈的所有獨立的同分異構體和所有含有線性或分支 7 個碳烷基鏈的 UVCB 物質 '4-Heptylphenol, branched and linear [substances with a linear and/or branched alkyl chain with a carbon number of 7 covalently bound predominantly in position 4 to phenol, covering also UVCB- and well-defined substances which include any of the individual isomers or a combination thereof]	-
172	十九氟癸酸及其鈉和銨鹽 Nonadecafluorodecanoic acid (PFDA) and its sodium and ammonium salts	3108-42-7 335-76-2 3830-45-3
173	對(1,1-二甲基丙基)苯酚 p-(1,1-dimethylpropyl)phenol	80-46-6
174	**全氟己基磺酸及其鹽類** Perfluorohexane-1-sulphonic acid and its salts (PFHxS)	355-46-4
175	1,2-苯并菲;(【艹快】) Chrysene	218-01-9
176	苯[a]蒽 Benz[a]anthracene	56-55-3
177	硝酸鎘 Cadmium nitrate	10325-94-7
178	氫氧化鎘 Cadmium hydroxide	21041-95-2
179	碳酸鎘 Cadmium carbonate	513-78-0
180	1,6,7,8,9,14,15,16,17,17,18, 18-十二氯五環 [12.2.1.16,9.02,13.05,10]十八碳-7,15-二烯 (“Dechlorane Plus” TM)[含有其任何單獨的反式和順式異構體或其任何組合] 1,6,7,8,9,14,15,16,17,17,18,18-Dodecachloropentacyclo[12.2.1.16,9.02,13.05,10]octadeca-7,15-diene(“Dechlorane Plus” TM) [covering any of its individual anti- and syn-isomers or any combinationthereof]	-
181	1,3,4-噻二唑-2,5-二硫醇與甲醛和支鏈和直鏈 4-庚基酚的反應產物(RP-HP) [含有≥ 0.1%w/w 支鏈和直鏈的 4-庚基酚] Reaction products of 1,3,4-thiadiazolidine-2,5-dithione,formaldehyde and 4-heptylphenol, branched and linear (RP-HP) [with ≥ 0.1%w/w 4-heptylphenol, branched and linear]	-

Original issue date: Jan. 15th, 2014

Declaration of Minerals Conflict-Free

Integrated Silicon Solution Inc., for and on behalf of itself and **Integrated Silicon Solution (Cayman), Inc.** (“**ISSI Cayman**”) and **Integrated Circuit Solution, Inc.**(“**ICSI**”) Chingis Technology Corporation (“Chingis”) (ISSI, ISSI Cayman, ICSI and Chingis hereinafter collectively referred to as “ISSI Groups”) declare that ISSI Groups do not to purchase and refuse to use conflict minerals, or their derivatives that may directly or indirectly finance or benefit armed groups through mining or mineral trading in the Democratic Republic of Congo (DRC) or an adjoining country.

“Conflict Minerals" are metals such as gold (Au), tantalum (Ta), tungsten (W) and tin (Sn) derived from minerals being sourced from mines in Democratic Republic of Congo (DRC) or an adjoining country (conflict areas) which are controlled by non-government military groups, or unlawful military factions the coverage on human rights violations in the Democratic Republic of the Congo (DRC) and environmental issues resulting from the extraction of minerals.

Integrated Silicon Solution Inc. will take due diligence within our supply chain to assure “DRC Conflict-Free”. Securities and Exchange Commission is adopting a new form and rule pursuant to Section 1502 of the Dodd-Frank Wall Street Reform and Consumer Protection Act relating to the use of conflict minerals. Section 1502 added Section 13(p) to the Securities Exchange Act of 1934, which requires the Commission to promulgate rules requiring issuers with conflict minerals that are necessary to the functionality or production of a product manufactured by such person to disclose annually whether any of those minerals originated in the Democratic Republic of the Congo or an adjoining country.

Integrated Silicon Solution Inc. would like to confirm Minerals used in Products sold to customers are “DRC Conflict-Free” and new form and rule pursuant to section 1502 of the Dodd-Frank Wall Street Reform and Consumer Protection Act.

Sincerely Yours,

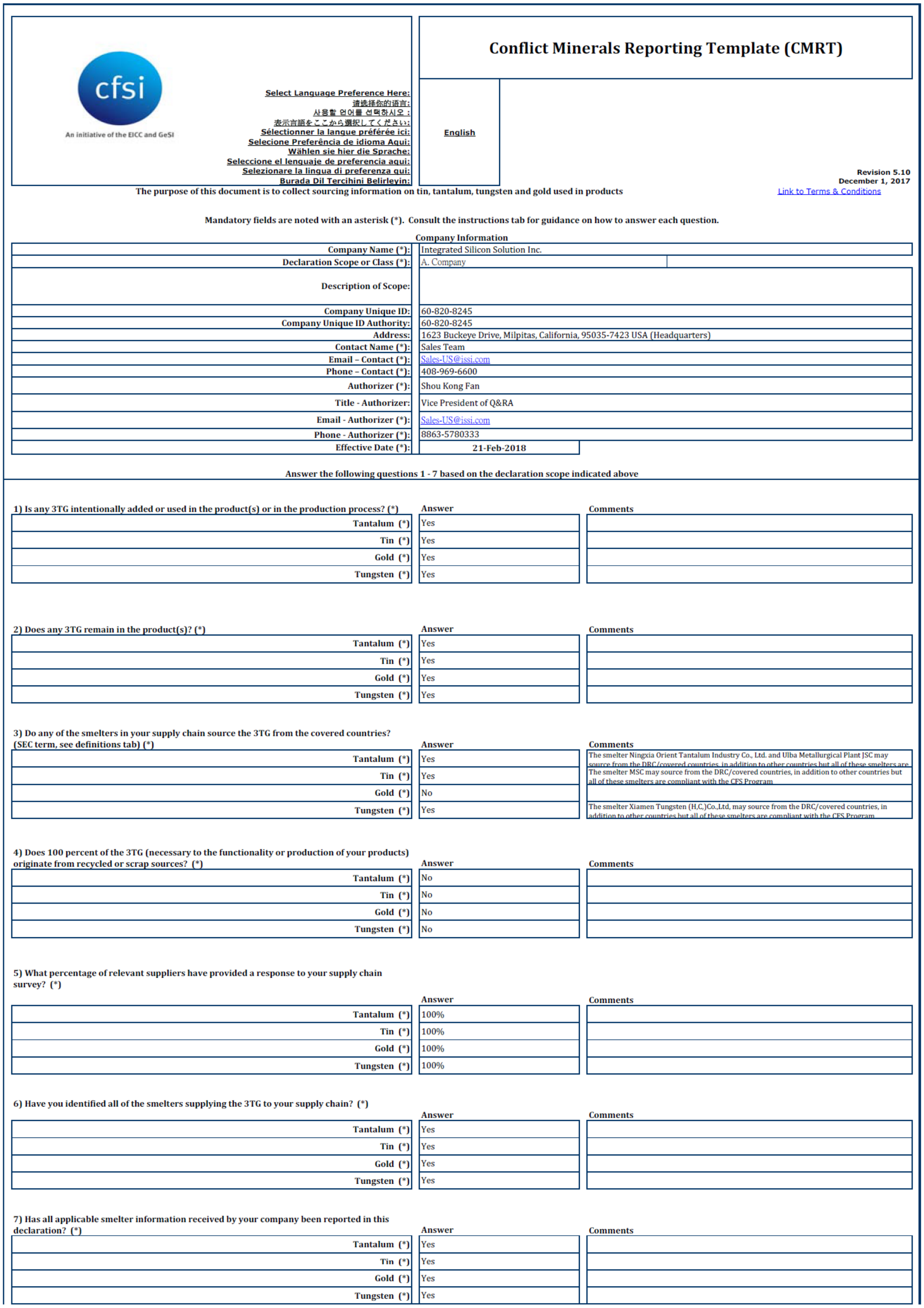
ShouKong Fan

Shou-kong Fan
Vice President
Quality & Reliability Assurance Division
Date: 2016/3/1

No.2, Technology Rd. V, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.

Tel: 886-3-5780333 Fax: 886-3-5783000 Web: **www.issi.com**

Conflict Free Materials Template (CMRT) for DRAM, SRAM, and Flash Memory



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Conflict Minerals Reporting Template (CMRT)

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Revision 5.10
December 1, 2017

The purpose of this document is to collect sourcing information on tin, tantalum, tungsten and gold used in products

Link to Terms & Conditions

Mandatory fields are noted with an asterisk (*). Consult the instructions tab for guidance on how to answer each question.

Company Information

Company Name (*):	Integrated Silicon Solution Inc.
Declaration Scope or Class (*):	A. Company
Description of Scope:	
Company Unique ID:	60-820-8245
Company Unique ID Authority:	60-820-8245
Address:	1623 Buckeye Drive, Milpitas, California, 95035-7423 USA (Headquarters)
Contact Name (*):	Sales Team
Email – Contact (*):	Sales-US@issi.com
Phone – Contact (*):	408-969-6600
Authorizer (*):	Shou Kong Fan
Title - Authorizer:	Vice President of Q&RA
Email - Authorizer (*):	Sales-US@issi.com
Phone - Authorizer (*):	8863-5780333
Effective Date (*):	21-Feb-2018

Answer the following questions 1 - 7 based on the declaration scope indicated above

1) Is any 3TG intentionally added or used in the product(s) or in the production process? (*)

	Answer	Comments
Tantalum (*)	Yes	
Tin (*)	Yes	
Gold (*)	Yes	
Tungsten (*)	Yes	

2) Does any 3TG remain in the product(s)? (*)

	Answer	Comments
Tantalum (*)	Yes	
Tin (*)	Yes	
Gold (*)	Yes	
Tungsten (*)	Yes	

3) Do any of the smelters in your supply chain source the 3TG from the covered countries? (SEC term, see definitions tab) (*)

	Answer	Comments
Tantalum (*)	Yes	The smelter Ningxia Orient Tantalum Industry Co., Ltd. and Ulba Metallurgical Plant JSC may source from the DRC/covered countries, in addition to other countries but all of these smelters are
Tin (*)	Yes	The smelter MSC may source from the DRC/covered countries, in addition to other countries but all of these smelters are compliant with the CFS Program
Gold (*)	No	
Tungsten (*)	Yes	The smelter Xiamen Tungsten (H,C,)Co.,Ltd, may source from the DRC/covered countries, in addition to other countries but all of these smelters are compliant with the CFS Program

4) Does 100 percent of the 3TG (necessary to the functionality or production of your products) originate from recycled or scrap sources? (*)

	Answer	Comments
Tantalum (*)	No	
Tin (*)	No	
Gold (*)	No	
Tungsten (*)	No	

5) What percentage of relevant suppliers have provided a response to your supply chain survey? (*)

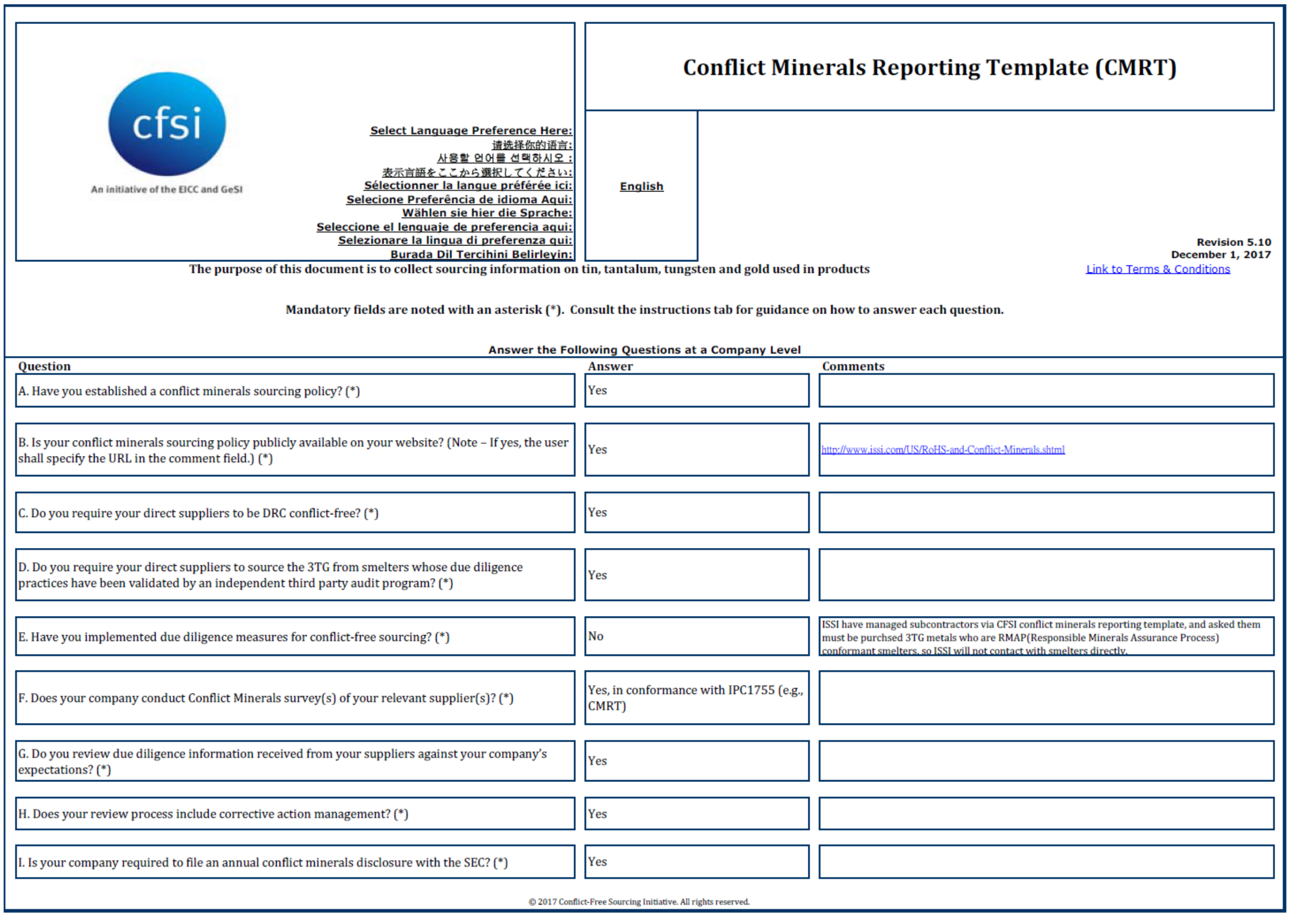
	Answer	Comments
Tantalum (*)	100%	
Tin (*)	100%	
Gold (*)	100%	
Tungsten (*)	100%	

6) Have you identified all of the smelters supplying the 3TG to your supply chain? (*)

	Answer	Comments
Tantalum (*)	Yes	
Tin (*)	Yes	
Gold (*)	Yes	
Tungsten (*)	Yes	

7) Has all applicable smelter information received by your company been reported in this declaration? (*)

	Answer	Comments
Tantalum (*)	Yes	
Tin (*)	Yes	
Gold (*)	Yes	
Tungsten (*)	Yes	



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Select Language Preference Here:
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表示言語をここから選択してください:
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Selecione Preferência de idioma Aqui:
Wählen sie hier die Sprache:
Seleccione el lenguaje de preferencia aqui:
Selezionare la lingua di preferenza qui:
Burada Dil Tercihini Belirleyin:

Conflict Minerals Reporting Template (CMRT)

English

Revision 5.10
December 1, 2017
Link to Terms & Conditions

The purpose of this document is to collect sourcing information on tin, tantalum, tungsten and gold used in products

Mandatory fields are noted with an asterisk (*). Consult the instructions tab for guidance on how to answer each question.

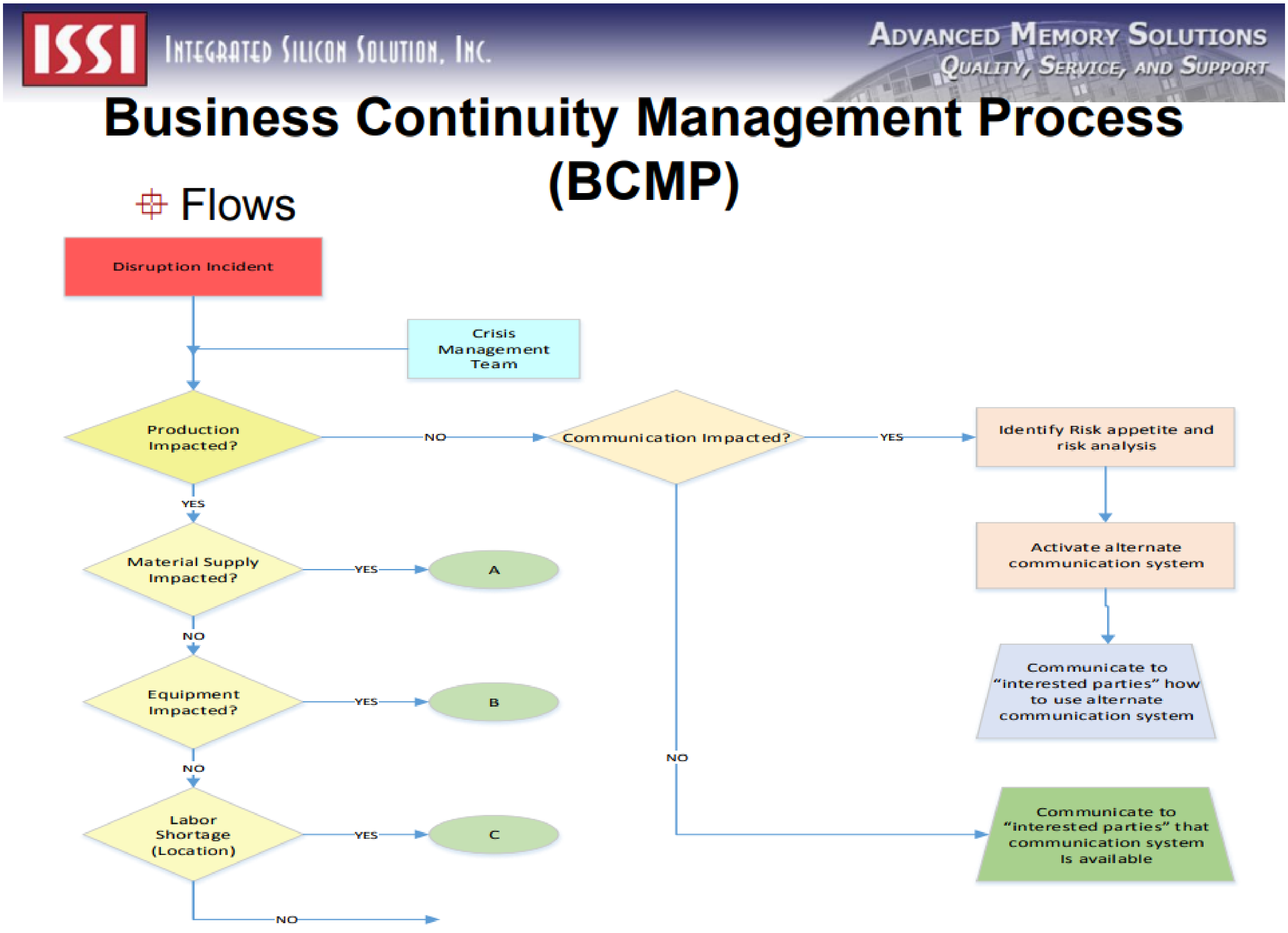
Answer the Following Questions at a Company Level

Question	Answer	Comments
A. Have you established a conflict minerals sourcing policy? (*)	Yes	
B. Is your conflict minerals sourcing policy publicly available on your website? (Note – If yes, the user shall specify the URL in the comment field.) (*)	Yes	http://www.issi.com/US/RoHS-and-Conflict-Minerals.shtml
C. Do you require your direct suppliers to be DRC conflict-free? (*)	Yes	
D. Do you require your direct suppliers to source the 3TG from smelters whose due diligence practices have been validated by an independent third party audit program? (*)	Yes	
E. Have you implemented due diligence measures for conflict-free sourcing? (*)	No	ISSI have managed subcontractors via CFSI conflict minerals reporting template, and asked them must be purchsed 3TG metals who are RMAP(Responsible Minerals Assurance Process) conformant smelters, so ISSI will not contact with smelters directly.
F. Does your company conduct Conflict Minerals survey(s) of your relevant supplier(s)? (*)	Yes, in conformance with IPC1755 (e.g., CMRT)	
G. Do you review due diligence information received from your suppliers against your company's expectations? (*)	Yes	
H. Does your review process include corrective action management? (*)	Yes	
I. Is your company required to file an annual conflict minerals disclosure with the SEC? (*)	Yes	

Please see http://www.issi.com/US/rohs.shtml for previous RoHS documents.

Business Continuity

ISSI has procedures for planning and implementing controls and measures to manage disruptive incidents and to monitor the effectiveness of these measures.



ISSI INTEGRATED SILICON SOLUTION, INC.

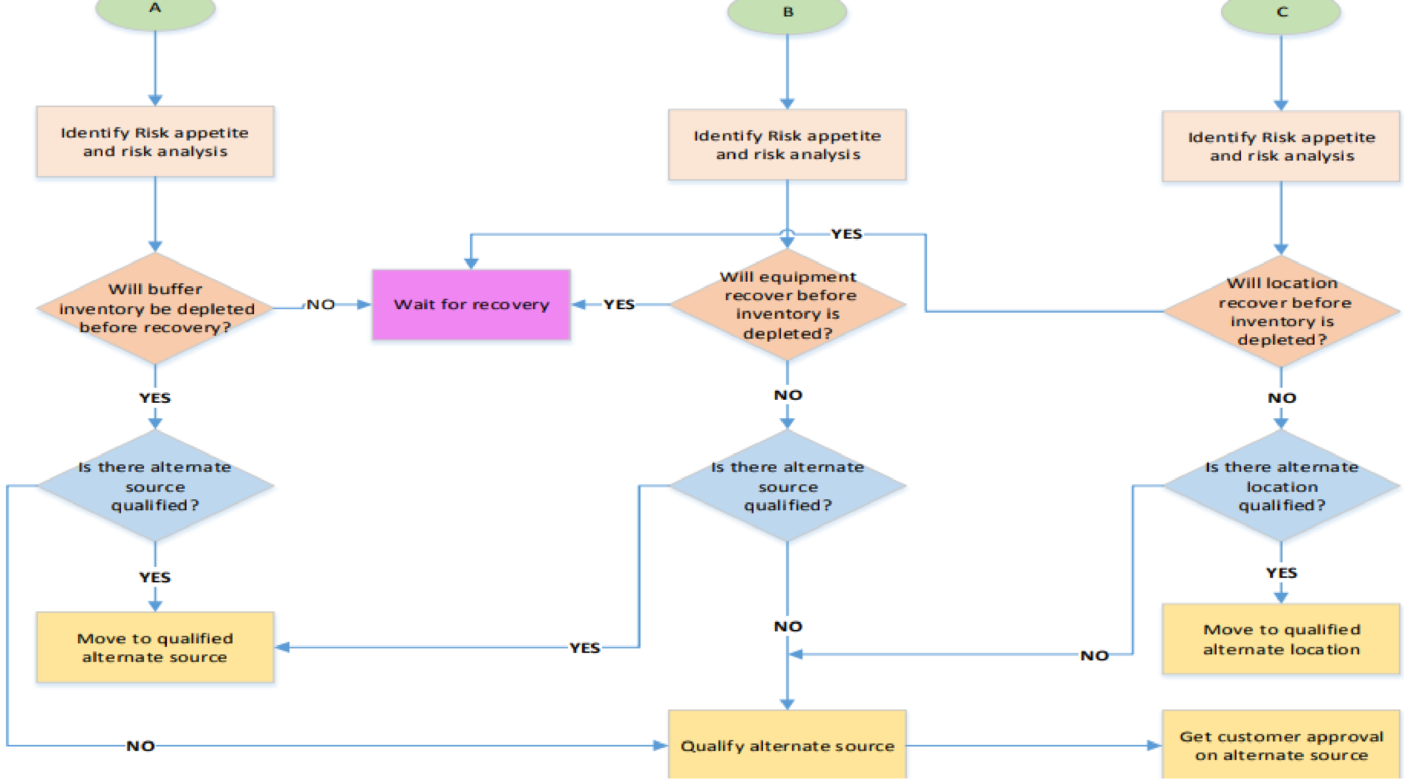
ADVANCED MEMORY SOLUTIONS
QUALITY, SERVICE, AND SUPPORT

Business Continuity Management Process (BCMP)

Flows

Business Continuity Management Process (BCMP)

- Flows (cont)



A

Identify Risk appetite and risk analysis

Will buffer inventory be depleted before recovery?

NO

Wait for recovery

YES

Is there alternate source qualified?

YES

Move to qualified alternate source

NO

B

Identify Risk appetite and risk analysis

YES

Will equipment recover before inventory is depleted?

YES

NO

Is there alternate source qualified?

YES

NO

Qualify alternate source

C

Identify Risk appetite and risk analysis

Will location recover before inventory is depleted?

NO

Is there alternate location qualified?

YES

Move to qualified alternate location

NO

Get customer approval on alternate source

Business Continuity Management Process (BCMP)

- Contingency plans for:
  - Material availability
  - Process continuance
  - Uninterrupted delivery
  - Continuous systems of communication
  - Replacement of lost parts

BCMP – ISSI Internal (Contingency plans per 230-110-005)

- Material availability
  - Wafers availability from foundry reviewed monthly and quarterly
  - Alternate sources reviewed for contingency
- Process continuance
  - Quarterly review of subcontractors for capability analysis and continuous supply
  - At any time during the week if there is any unscheduled interruption, the Risk Management team shall meet and make decisions on alternative sources
- Uninterrupted delivery
  - Alternative means of delivery are set up for different locations.

BCMP – ISSI Suppliers (Fab and Subcon)

- Material availability
  - Purchasing monitors wafer deliveries
  - Buffer inventory prepared to ensure supply
- Process continuance
  - Equipment consignment to key subcontractors guarantee continuous supply in case of process interruption in one location
  - Joint investment and Financial support of Fab and subcon guarantee priority of material supply in case of interruption
  - Qualified alternative subcontractor
- Uninterrupted delivery
  - Alternative means of delivery are set up for different locations.