

ISSI LPDDR4 SDRAM Layout Guide

Application Note (AN43LQ001)

Introduction

This is a general PCB layout guideline for ISSI LPDDR4 SDRAM, especially targeting point-to-point applications. Chipset companies may require special or additional guidelines for LPDDR4. In these cases, ISSI recommends that the Chipset company's guidelines should be applied first.

PCB Layout Guidelines

FR-4 is commonly used as a dielectric material. Thickness and trace widths should be adjusted for optimal impedance. Propagation delays and trace lengths are also important and should be confirmed with simulations for each signal group. In general, ISSI recommends minimum design rules for PCB layout as defined below for peak performance and to minimize signal distortion/crosstalk.

1. Signals from the same Byte group, such as DQS, DMI and bits of DQ, should be routed in the same layer if possible. If a layer transition is necessary, return current paths should be minimized to reduce inductance and impedance discontinuities. Optimizing Stitching VIAs and Bypass Capacitors will also help to minimize impedance discontinuities which reduces crosstalk and signal distortion.
2. The DQ/DMI/DQS signals must be routed in inner layers as stripline or embedded microstrip. They need to follow the 3W rule (center-to-center) with the same number of VIAs and barrel lengths to minimize trace crosstalk. DQ and DMI traces are recommended to be controlled to approximately 40Ω instead of 50Ω , for optimal timing margins. Stubs/Branches should not be used for signal access in any Data groups.
3. Propagation (Trace) delay must be carefully evaluated and controlled for the respective groups. Package delays should also be included in simulations to ensure timing budgets have adequate margin in the application.
4. The following table is a good guideline for propagation delay considerations.

LPDDR4 signal(each 16-bit channel)	Group	PCB + package prop delay		Considerations
		Min	Max	
CK_t/CK_c	Clock	Short as possible	180ps	Match the true/complement signals within 1ps
CA[5:0]	Address/Command/Control	CK_t - 25 ps	CK_t + 25 ps	
CS				
CKE				
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 85 ps	CK_t + 85 ps	Match the true/complement signals of DQS within 1ps
DM0	Byte 0 - Data	DQS0_t - 10 ps	DQS0_t + 10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 85 ps	CK_t + 85 ps	
DM1	Byte 1 - Data	DQS1_t - 10 ps	DQS1_t + 10 ps	
DQ[15:8]				

- Chipset vendors require that the LPDDR4 package be placed within a certain length of the memory controller. Please contact the chipset vendor about this. In general, 100 mils (2.5mm) is a reasonable distance.
- Minimum trace width is 4mil (0.1mm).
- Intranet spacing, the distance between two adjacent traces within a net, is 8mil (0.2mm).
- Internet spacing, the distance between the two outermost signals of different signal group is 20mil (0.5mm).
- Single ended impedance on PCB: $39\Omega \pm 10\%$
- Clock differential impedance on PCB : $76\Omega \pm 10\%$
- Clocks should be routed on top layer for optimal signal quality without VIA's and maintain >5W spacing from other signals.
- Differential clocks should be routed in parallel and keep the trace length as short as possible.
- LPDDR4 offers programmable drive strength to match the impedance of IO BUS. Six drive strengths are supported: RZQ/6,RZQ/5,RZQ/4,RZQ/3,RZQ/2 and RZQ/1. This feature can avoid using any termination of IO BUS to help improve power consumption and minimize space.
- The LPDDR4 RZQ feature minimizes any process variation present in the driver. To calibrate output driver impedance, RZQ needs to be located between the ZQ ball and VDDQ. The value of RZQ must be $240\Omega \pm 1\%$.
- ISSI recommends that the RESET_n pin on LPDDR4 is tied to GND through a 4.7K Ω resistor.
- ISSI recommends that each ODT_CA pin on LPDDR4 is tied to VDD2 through a 4.7K Ω resistor.
- Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. For high-speed bypassing, select the required capacitance with the smallest package.

LAND pattern

Follow IPC-7351, to keep size of land patterns to be equal to 80% of the ball size of BGA.

For any questions, please contact the following individuals from [ISSI Application Engineering Department](#).