AN43QR001.AN

ISSI DDR4 SDRAM Layout Guide

Application Note (AN43QR001)

Introduction

This is a general PCB layout guideline for ISSI DDR4 SDRAM, especially for point-to-point applications. Chipset companies may have additional guidelines or requirements to use DDR4 with their DRAM controller. In such cases, ISSI recommends that those guidelines serve as primary, while these guidelines be considered as supplementary.

It is strongly encouraged that the board designer(s) consider all aspects of the board, such as signal integrity, electrical timings, etc., by using simulation models prior to board fabrication. After the board has been produced and completed with components, it is also recommended to further verify signal integrity and full functionality of the application.

PCB Layout Guidelines

FR-4, is commonly used as a dielectric material. The thickness and trace widths should be adjusted for optimal impedance. Propagation delays and trace lengths are also important and should be confirmed with simulations for each signal group. In general, ISSI recommends minimum design rules for PCB layout as defined below, for peak performance and to minimize signal distortion/crosstalk.

1. Decoupling Guidelines:

Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure the high-speed transient current required by the processor. For high-speed bypassing, select the required capacitance with the smallest package. The table below is the summary of power line design considerations.

	General Guideline	Other notes
VDD	25uF of capacitance can be provided for each DRAM device placement. Minimum of two decoupling capacitors to VSS per SDRAM.	Should be placed as close as possible to the DRAM VDD balls. Small-value capacitors with more placements are preferred.
VTT	Connect 0.1uF decoupling capacitor for every two termination resistors. Use at least one 4.7 µF capacitors at each end of the VTT island.	Make VTT voltage decoupling close to the components and pull-up resistors. Use a wide surface trace (~150 mils) for the VTT island trace.
VPP	2-3uF of capacitance for each DRAM device is recommended to supply the burst Vpp current. Stagging two to three 1.0uF capacitors near the VPP pins may reduce the high-frequency power noise better.	Should be placed as close as possible to the DRAM VPP ball. The VPP supply is ramped before or at the same time as the VDD supply.
VREFCA	A minimum of one 0.1uF decoupling capacitor to GND or VDD based on the reference plane is needed.	Should be placed as close as possible to the DRAM VREFCA ball. VREFCA should be isolated from noisy aggressors with maintaining at least a 20–25 mils clearance from other traces.

Note1. Decoupling capacitor values vary by application and may be staggered to achieve the best overall impedance vs. frequency response.

Note2. Recommended values for decoupling are 0.01uF, 0.1uF, and 1.0uF.

Note3. The recommended value for a bulk capacitor is 4.7uF.

2. Signal Groups:

Signal Groups are:

2.1 Clock (CK)

2.2 Address, Bank Address, Bank Group, Command and Control (ADD/CMD/CTRL)

2.4 Data Bus (including ECC byte) (DQ)

3. Trace length and matching rules:

The fly-by routing is recommended for address, command, control, and clock signal bus. The below table shows the length and matching rules for each signal group.

Group	PCB + package prop delay		Considerations
	Min	Max	
Clock(CK)	Short as possible	180ps*1	Match the true/complement signals within 0.5%(=+-0.25%) of the clock period or ±2ps. Clocks should maintain a length-matching between clock pairs of ±5 ps.
Address/Command/ Control	CK_t - 20 ps	CK_t + 20 ps	Route all addresses and commands to match the clock signals to within ±20 ps to each DDR4 component
Data Bus within the byte lane group (DQS, DQs, DMs)	DQS0_t - 10 ps	DQS0_t + 10 ps	Match in length all DQ, DQS, and DM signals within a given byte-lane group with a maximum deviation of ±10 ps. Match the true/complement DQS signals within 0.5%(=+-0.25%) of the clock period or ±2ps.

Note 1. The maximum trace length requirement can vary by the controller. Please refer to the controller's layout guideline.

4. Impedance Assignments by Signal Type:

4.1 Signals from the same Byte group, such as DQS, DM and bits of DQ, should be routed in the same layer, if possible. If a layer transition is necessary, return current paths should be minimized to reduce inductance and impedance discontinuities. Optimizing Stitching VIAs and Bypass Capacitors will also help to minimize impedance discontinuities, which reduces crosstalk and signal distortion.

4.2 The DQ/DMI/DQS signals must be routed in inner layers with the same number of VIAs and barrel lengths to minimize trace crosstalk. DQ and DMI traces are recommended to be controlled to ~40Ω

4.3 Propagation (Trace) delay must be carefully evaluated and controlled for the respective groups. Package delays should also be included in simulations to insure timing budgets have adequate margin in the application.

4.4 Trace impedance recommendations & thickness:

Signal Type	Impedance	Trace Width	
		Minimum	Nominal
CLOCK	70 Ω differential	0.1mm	0.15mm - 0.25mm
ADD/CMD/CTRL	40 Ω	0.1mm	0.15mm
DQ	40 Ω	0.1mm	0.15mm
DQS	83 Ω	0.1mm	0.15mm

Impedances for DDR4:

4.4.1 40 Ω ± 10% (nominally achieved with 0.15 mm trace widths)

Differential impedances for DDR4:

4.4.2 83 Ω ± 15% (nominally achieved with 0.10 mm trace widths with a 0.10 mm space)

4.4.3 70 Ω ± 15% (nominally achieved with 0.15 mm trace widths with a 0.10 mm space)

4.5 The chipset manufacturer requires that each DDR4 package be located within a certain length. Please contact the chipset vendor for further details.

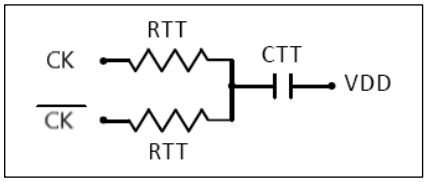
5. Routing Space Constraints:

Feature	Preferred (mm)	Comment
Pad to pad spacing for pads of different components that are soldered down	0.250	The concern is solder bridging
Line to pad spacing	0.125	
Line to line spacing (single ended)	0.100	
Line to line spacing (differential)	0.100	
Line to shape spacing	0.200	
Shape to shape spacing	0.200	
Via to BGA pad	0.175	Copper to copper
Via to non-BGA pad	0.150	Copper to copper
Via to Via	0.200	Copper to copper
Minimum trace width on outer layers	0.090	
Minimum trace width on inner layers	0.075	

5.1 Clocks should be routed on the top layer for optimal signal quality without VIA's. They should maintain >5W spacing from other signals.

5.2 Differential clocks should be routed in parallel, with trace lengths as short as possible.

5.3 Terminations for differential clocks will use two resistors, one connected to each side: the true signal and the complementary signal for the differential pair. The other side of each resistor should be connected together and to a capacitor. The other side of the capacitor will be connected to the reference plane for the differential pair. This will be VDD and the capacitor value should be 0.01 µF to 0.1 µF.



5.4 DDR4 offers programmable drive strength to match the impedance of I/O BUS. Seven drive strengths are supported: RZQ/7, RZQ/6, RZQ/5, RZQ/4, RZQ/3, RZQ/2 and RZQ/1.
This feature can avoid using any termination of I/O BUS to help improve power consumption and conserve space.

5.5 The DDR4 RZQ feature minimizes process variations that may be present in the driver. To calibrate output driver impedance, RZQ needs to be located between the ZQ ball and VSSQ. The value of RZQ must be 240Ω ±1%.

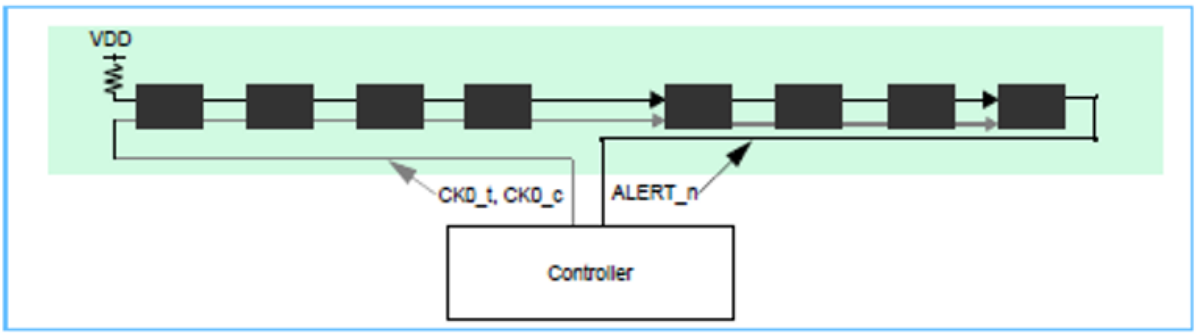
5.6 ISSI recommends that the RESET pin on DDR4 is tied to VSS through an appropriate value resistor for the number of loads to maintain 0.2 x VDD during power up.

5.7 ISSI recommends that the ODT pin on DDR4 be tied to VTT through a 33Ω - 39Ω resistor.

5.8 ISSI recommends if CA Parity feature is used, terminate PAR pin to VTT through a 33Ω - 39Ω resistor.

5.9 ISSI recommends that the TEN pin on DDR4 be tied to GND through a 1K Ω resistor.

5.10 ISSI recommends that ALERT# pin on DDR4 be tied to VDD through a 1K Ω or 4.7K Ω resistor after the last DRAM connection (see diagram below).



6. LAND pattern

Follow IPC-SM-782 and IPC-7351, and target the size of land pattern to be equal to 80% of the ball size of BGA.

For any question, please contact the ISSI Application Team.