

ISSI DDR3 SDRAM Layout Guide

Application Note (AN43TR001)

1. Introduction

This is a general PCB layout guideline for ISSI DDR3 SDRAM, especially targeting point-to-point applications. DDR3 is an evolutionary transition from the previous memory generation, DDR2. DDR3 allows clock frequencies and data bandwidth to be more than double that of DDR2, while adding other features that simplify the layout of memory and improve signal integrity. These features include on-the-fly calibration to adjust for voltage and temperature variations to maintain stable Output drive characteristics, On-Die termination (ODT) with dynamic control and additional advanced capabilities that are well suited for point-to-point applications. The manufacturers of Systems-on-Chip (SoC), MPU, and other devices with a DDR3 memory controller are likely to specify limits, requirements, or recommendations in using their devices with DDR3. As such, ISSI recommends that the user apply those guidelines as the primary reference, while ISSI's DDR3 layout guideline be considered as supplementary. The ISSI datasheet for the specific DDR3 product being implemented should always be an important reference, with the user making sure that there is no violation.

It is strongly encouraged that the board designer(s) consider all aspects of the board, such as signal integrity, electrical timings, etc., by using simulation models such as IBIS prior to board fabrication. After the board has been produced and completed with components, it is also recommended to further verify signal integrity and full functionality of the application with the selected ISSI DDR3 DRAM.

2. PCB Layout Guidelines

FR-4 is commonly used as a dielectric material. Thickness and trace widths should be adjusted to match the desired impedance. Trace lengths are also important and their impact on performance should be confirmed in simulations for each of the critical clock and net groups. Generally, single impedances (CA, Control & DQ's) are 50Ω (+/- 10%) and differential impedances (Clocks, DQS's) are nominally 100Ω (+/- 10%) and are typically routed on inner layers if possible. In slower applications, crosstalk issues would be less and closer spacing may be allowed after careful simulation to evaluate the design rule changes. Minimum spacing guidelines in these examples are dependent on dielectric thickness, routing pitch and should be verified with simulations to reduce intranet/internet group coupling/crosstalk. All impedances should be verified and monitored for each layer to make sure they comply with design specifications.

3. Power Distribution

As clock frequencies increase, power distribution networks (PDN) must be carefully controlled to insure adequate timing margin and noise immunity. This is especially critical in wide I/O designs where simultaneous switching of the outputs (SSO) is common. In this case, power distribution networks can experience large peak current

demands on Vddq and Vssq lines. If the power network isn't carefully designed, peak current demand (High Drive Strength) can negatively impact timing margins and in extreme cases cause power supply deficiencies. Supply and ground planes, routing and decoupling should be checked to ensure optimal voltage/current supply for DDR3 devices.

The following are general guidelines for PDN development in DDR3 board designs.

1. Solid Power and Ground planes should be used in DDR3 routing areas.
2. Place a 0.1uF cap and 0.01uF as close as possible for every VDDQ pin.
3. VTT decoupling should be as close to the components and pull-up resistors as possible.
4. Place a 0.1uF decoupling cap between VTT and VDD.
5. Low ESL decoupling capacitors should be used, and routing should be carefully evaluated to minimize inductance.
6. Power connections from supply planes to vias for device pins or decoupling capacitors should be as short (<8 mils) and as wide as possible (trace widths should be the same or larger than the via size) to minimize trace impedance.

A hierarchical design approach is recommended in DDR3 board layout with differential clocks (CK/CK#) and Data Strobes (DQS/DQS#). Overall routing lengths for these signals (CK/CK# & DQS/DQS#) should be matched within ± 2 ps or a maximum of 10mils between true and compliment signals. Route the CK/CK# clocks and set as the target trace propagation delays for the DQ net group. Match the CK/CK# clock to within ± 5 ps of all DQS/DQS#. DQ and DM net groups should be routed with their respective DQS/DQS# and DM on the same PCB layer and matched within ± 10 ps, with a maximum difference of 50mils. DQS/DQS# should be used as the target trace propagation delay for the associated Data and data mask signals.

Ideally, route the address/control signal group on the same layer as the CK/CK# clocks, and keep within ± 10 ps skew of the CK/CK# traces. The following table shows recommended baseline specifications at the beginning of a board design. The values in this table are general guidelines and should be confirmed with board simulations to verify design targets and operating margins.

Signals on Net	Maximum deviation of signal propagation difference.	Maximum deviation of trace length.
Between signals within byte group (DQS, DM, 8bits of DQ)	± 10 ps	± 1.270 mm(50mil)
Between signals within address net. Between signals within commands net. Between one byte group and another byte group.	± 50 ps	± 6.635 mm(261mil)
Between CK and CK#. Between DQSn and DQS#n	± 2 ps	± 0.254 mm (10mil)
Between one clock pair and another clock pair, eg: CK/CK# and DQSn/DQS#n.	± 5 ps	± 0.635 mm(25mil)

Notes:

1. Minimum trace width is 0.13mm (5mil).
2. Intranet spacing, the distance between two adjacent traces within a net, is 8mil (depending on dielectric thickness)
3. Internet spacing, the distance between the two outermost signals of different signal groups is 15mil. The same rule applies between one clock pair and another clock pair.
4. Differential clocks should be routed in parallel with short trace lengths.
5. Differential clocks must be routed on the same layer and placed on an internal layer to minimize the noise.
6. Due to crosstalk and signal noise reduction, keep the trace lengths as short as possible. ISSI recommends less than 20mm.
7. Signals from the same net group should be routed on the same layer.
8. Signals from the same Byte group, such as DQS, DM, and 8 bits of DQ, must be routed in the same layer.
9. The restriction between the clock pair and the DQS pair can be waived if the system performs a calibration to account for the delay.

10. V_{REF} Control

V_{REF} should be designed to provide optimum noise margin in the system. V_{REF} levels must be carefully controlled and isolated from noise conditions to prevent potential timing errors which can reduce setup and hold time margins, increase jitter, and cause erratic memory bus behavior. V_{REF} is expected to track variations in V_{DDQ} , and the peak-to-peak noise must remain within specification.

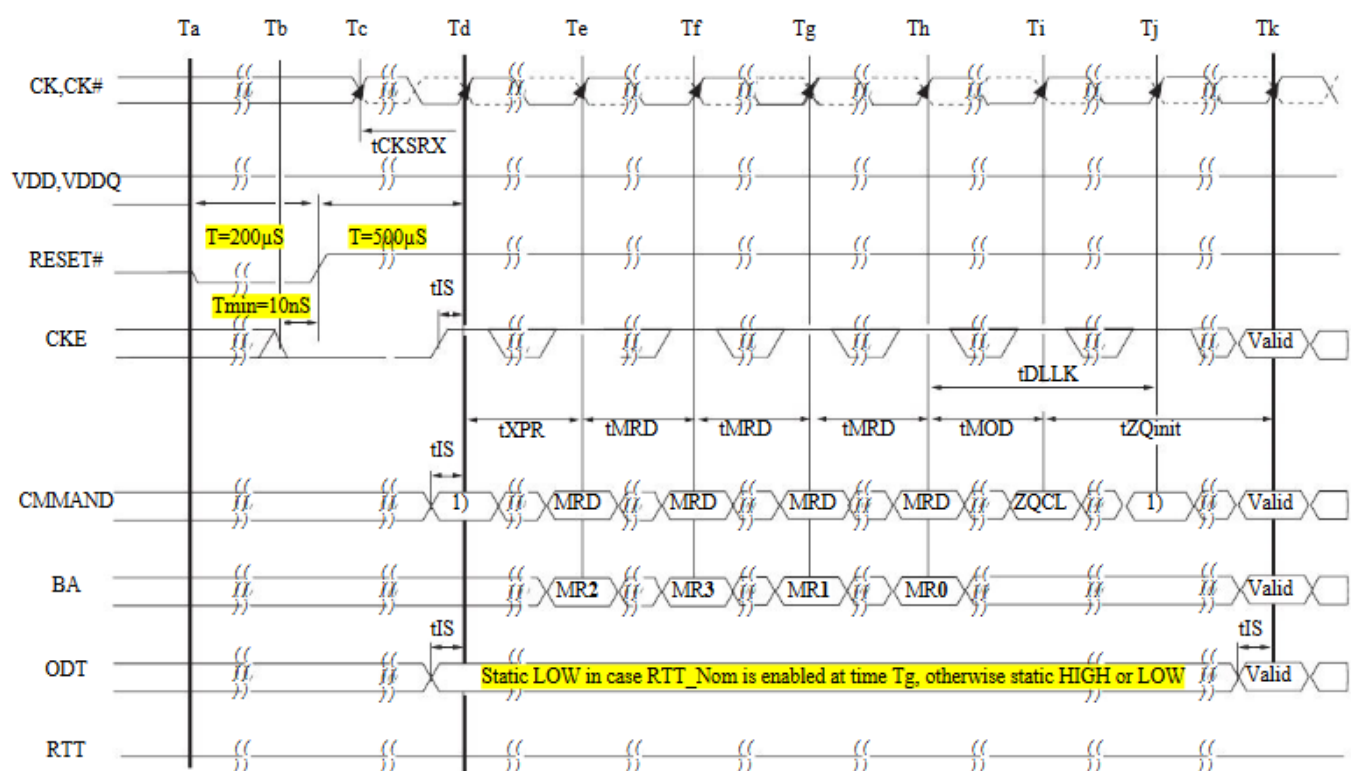
1. Place a 0.1uF capacitor between V_{REF} and V_{DDQ}
2. Place a 0.1uF capacitor between V_{REF} and V_{SSQ}
3. V_{REF} should have a minimum trace length to reduce inductance.
4. V_{REF} should have a wide trace. Min 20 mil is recommended.
5. V_{REF} should maintain a minimum of 25mil width and spacing from other signals to minimize coupling effects and ideally be isolated with adjacent ground traces.
6. Each V_{REF} source and destination should be decoupled with 0.1uF caps.

7. EMI and Termination

The DDR3 SDRAM uses a programmable impedance output buffer. The output drive strength is calibrated during initialization, which minimizes any process variation present in the driver. To calibrate output driver impedance, RZQ needs to be located between the ZQ ball and VSSQ. The value of RZQ must be $240\Omega \pm 1\%$ and can't be shared—each DDR3 should have its own RZQ. Drive strength is selected by programming specific bit values in the Memory Mode Register 1 (MR1). The default strength is $RZQ/6 (=40\Omega)$. During layout, the impedance for all single ended data groups is approximately 50Ω and differential signals are nominally 100Ω . Refer to the design guideline by the manufacturer of DDR3 memory controller for any restrictions or recommendations.

8. Initialization

Similarly to other DRAM, DDR3 has extensive features, which requires that the user carefully adhere to the power-up and initialization routines. When the DDR3 memory is powered up, the device follows its designed routine to initialize the internal state machines and to configure the numerous user-defined operating options. When power is ramped, the RESET# input should be maintained below $0.2 \times VDD$. To assure the proper state of this signal, ISSI recommends connecting RESET# with a pull-down resistor of value 1K Ω . Holding the RESET# pin Low ensures that all outputs remain disabled (High-Z) and that ODT is off (Rtt is High-Z). Until the power supplies are stable, RESET# Low should be maintained to ensure the outputs remain disabled (High-Z). Following a stable power supply condition, RESET# must be LOW for at least 200 μ s to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH. CKE must be LOW 10ns prior to RESET# transitioning HIGH. After RESET# transitions HIGH, wait 500 μ s with CKE LOW. The power voltage ramp time between 300mV to VDD (min) must be no greater than 200ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts. Refer to the respective ISSI DDR3 datasheet for the complete Initialization procedure.



Note1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Time Rest DON'T CARE

Reset and Initialization Sequence at Power-on Ramping (Figure from ISSI DDR3 Datasheet)

9. Land pattern

Follow IPC-7351, keep size of land pattern to be equal to 80% of the ball size of BGA.

For any question, please contact the [ISSI Application Team](#)