Errata: OctalRAM/HyperRAM/QuadRAM Requirements Update

2/1/2023

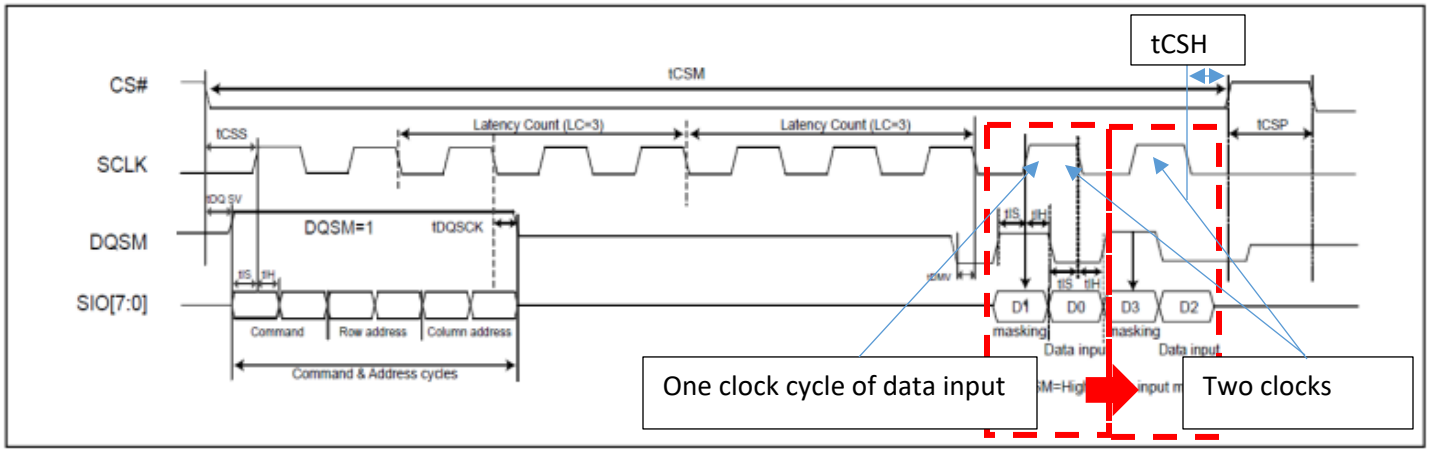
Scope of the products

IS66WVQ2M4DALL, IS67WVQ2M4DALL, IS66WVQ2M4DBLL, IS67WVQ2M4DBLL, IS66WVQ2M4EDALL, IS67WVQ2M4EDALL, IS66WVQ2M4EDBLL, IS67WVQ2M4EDBLL, IS66WVQ4M4DALL, IS67WVQ4M4DALL, IS66WVQ4M4DBLL, IS67WVQ4M4DBLL, IS66WVQ4M4EDALL, IS67WVQ4M4EDALL, IS66WVQ4M4EDBLL, IS67WVQ4M4EDBLL, IS66WVQ8M4DALL, IS67WVQ8M4DALL, IS66WVQ8M4DBLL, IS67WVQ8M4DBLL, IS66WVO8M8DALL, IS67WVO8M8DALL, IS66WVO8M8DBLL, IS67WVO8M8DBLL, IS66WVO8M8EDALL, IS67WVO8M8EDALL, IS66WVO8M8EDBLL, IS67WVO8M8EDBLL, IS66WVO16M8DALL, IS67WVO16M8DALL, IS66WVO16M8DBLL, IS67WVO16M8DBLL, IS66WVO16M8EDALL, IS67WVO16M8EDALL, IS66WVO16M8EDBLL, IS67WVO16M8EDBLL, IS66WVO32M8DALL, IS67WVO32M8DALL, IS66WVO32M8DBLL, IS67WVO32M8DBLL, IS66WVO64M8DALL, IS67WVO64M8DALL, IS66WVO64M8DBLL, IS67WVO64M8DBLL, IS66WVH8M8DALL, IS67WVH8M8DALL, IS66WVH8M8DBLL, IS67WVH8M8DBLL, IS66WVH8M8EDALL, IS67WVH8M8EDALL, IS66WVH8M8EDBLL, IS67WVH8M8EDBLL, IS66WVH16M8DALL, IS67WVH16M8DALL, IS66WVH16M8DBLL, IS67WVH16M8DBLL, IS66WVH16M8EDALL, IS67WVH16M8EDALL, IS66WVH16M8EDBLL, IS67WVH16M8EDBLL, IS66WVH32M8DALL, IS67WVH32M8DALL, IS66WVH32M8DBLL, IS67WVH32M8DBLL, IS66WVH64M8DALL, IS67WVH64M8DALL, IS66WVH64M8DBLL, IS67WVH64M8DBLL

It has been brought to our attention that the current OctalRAM/HyperRAM/QuadRAM when operating in variable latency mode, requires a minimum of two cycles of data inputs for proper functioning. This requirement was not previously specified in the product datasheet, and we apologize for any confusion this may have caused.

From the datasheet, tCSH is there to guide the CS# diassertion to be done "after" the clock falling edge. So, the minimum data size requirement becomes 16 bits for OctalRAM and HyperRAM and 8 bits for QuadRAM, which can be done with one clock pulse.

Figure 5.6 Refresh Collision at Variable Latency WRITE (2LC) / Data Input Masking



However, the current version requires one more cycle to finish the write operation safely. For example, all D0-D3 inputs from Figure 5.6 must be issued to ensure the device's proper operation. Please note that this issue will be resolved in the new batch of OctalRAM devices, and future shipments will not be affected.

Workaround solutions

Customers may choose to operate the device in fixed latency mode as a workaround solution or set the minimum data input size to 32 bits.